JC574 U.S. PTO
03/20/98

S&H Form: PTO/SB/05 (12/97)

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	122.1329
First Named Inventor or Application Identifier:	Hisanori FUJISAWA
Express Mail Label No.	

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form
2. [X] Specification, Claims & Abstract ..... [Total Pages: 34]
3. [X] Drawing(s) *(35 USC 113)* ..... [Total Sheets: 14]
4. [X] Oath or Declaration ..... [Total Pages: 3]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)*
      i. [ ] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation by Reference (usable if Box 4b is checked)
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. [ ] Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, status still proper and desired.
15. [X] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other:

17. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: ___/_____

18. CORRESPONDENCE ADDRESS

STAAS & HALSEY
Attn: H. J. Staas
700 Eleventh Street, N.W., Suite 500
Washington, DC 20001

Telephone: (202) 434-1500
Facsimile: (202) 434-1501

© 1997 Staas & Halsey

S&H Form (2/98)

NEW APPLICATION FEE TRANSMITTAL

		Attorney Docket No.	122.1329
		Application Number	
		Filing Date	March 20, 1998
AMOUNT ENCLOSED	$ 830.00	First Named Inventor	Hisanori FUJISAWA

FEE CALCULATION (fees effective 10/01/97)

CLAIMS	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS	8 - 20 =	0	X $ 22.00 =	$ 0.00
	INDEPENDENT CLAIMS	2 - 3 =	0	X $ 82.00 =	0.00
	MULTIPLE DEPENDENT CLAIMS (any number; if applicable)			+ $270.00 =	0.00
				BASIC FILING FEE	+ 790.00
				Total of above Calculations =	$ 790.00
	Surcharge for late filing fee, Statement or Power of Attorney ($130.00)				+ 0.00
	Reduction by 50% for filing by small entity (37 CFR 1.9, 1.27 & 1.28).				- 0.00
				TOTAL FILING FEE =	$ 790.00
	Surcharge for filing non-English language application ($130.00; 37 CFR 1.52(d))				+ 0.00
	Recordation of Assignment ($40.00; 37 CFR 1.21(h)(1))				+ 40.00
				TOTAL FEES DUE =	$ 830.00

METHOD OF PAYMENT

[X] Check enclosed as payment.

[ ] Charge "TOTAL FEES DUE" to the Deposit Account No., below.

[ ] No payment is enclosed and no charges to the Deposit Account are authorized at this time.

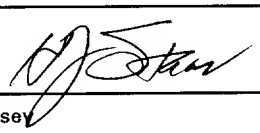
GENERAL AUTHORIZATION

[X] If the above-noted "AMOUNT ENCLOSED" is not correct, the Commissioner is hereby authorized to credit any overpayment or charge any additional fees necessary to:

Deposit Account No.	19-3935
Deposit Account Name	STAAS & HALSEY

[X] The Commissioner is also authorized to credit any overpayments or charge any additional fees required under 37 CFR 1.16 (filing fees) or 37 CFR 1.17 (processing fees) during the prosecution of this application, including any related application(s) claiming benefit hereof pursuant to 35 USC § 120 (e.g., continuations/divisionals/CIPs under 37 CFR 1.53(b) and/or continuations/divisionals/CPAs under 37 CFR 1.53(d)) to maintain pendency hereof or of any such related application.

SUBMITTED BY: STAAS & HALSEY

Typed Name	H. J. Staas	Reg. No.	22,010
Signature		Date	March 20, 1998

© 1997, 1998 Staas & Halsey

METHOD AND APPARATUS FOR CARRYING OUT CIRCUIT SIMULATION

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method and apparatus for carrying out circuit simulation which simulates, at high speed, a circuit that is an object of circuit simulation.

In particular, the present invention relates to a circuit simulation technique for simulating and inspecting a MOS large-scale integrated (abbreviated to LSI) circuit, which includes a plurality of MOS semiconductor devices, as an object of circuit simulation, and for thus checking if the MOS LSI circuit satisfies design specifications or for improving the performance of the MOS LSI circuit.

2. Description of the Related Art

For simulating a circuit to be simulated using a circuit simulator or the like, a current flowing into each terminal in the circuit or a voltage at the terminal are calculated on the basis of the connectional relationship of each modeled circuit element in the circuit, the characteristics of the modeled circuit element, and the connectional relationship of an input terminal of the circuit to be simulated. In this case, when the circuit to be simulated is handled as it is and simulated, it takes too much time for the simulation. It is hard to achieve circuit simulation efficiently in a short period of time. In particular, a MOS LSI circuit is large in scale. In the circumstances, it is required that the circuit to be simulated is simplified while the accuracy in operation of the circuit is ensured, and thus the time required for simulation is shortened in order to carry out simulation at high speed.

For a better understanding of the problem lying in a circuit simulation method in accordance with a

related art, the circuit simulation method and a circuit to be simulated will be described with reference to Figs. 1A, 1B and 2 that will be referred to in "Brief Description of the Drawings."

Figs. 1A and 1B are flowcharts each describing an example of a circuit simulation method in accordance with the related art; and Fig. 2 is a circuit diagram showing a typical example of a circuit to be simulated which will be compressed according to the circuit simulation method described in Figs. 1A and 1B.

For brevity's sake, a signal delay circuit composed of two n-type MOS (NMOS) transistors as shown in a portion (A) of Fig. 2, and a logic circuit composed of three NMOS transistors as shown in a portion (C) of Fig. 2 will be discussed as the circuit to be simulated. A circuit including one NMOS transistor as shown in a portion (B) of Fig. 2 is, as described later, a compressed form of the signal delay circuit shown in the portion (A) of Fig. 2.

The circuit simulation method shown in Figs. 1A, 1B and 2 has been disclosed in, for example, the specification of a patent application of the related art (Japanese Patent Application No. 8-198074 filed on July 26, 1996) filed by the same inventor and applicant as those of this application.

In the flowchart of Fig. 1A, first, a net Ni (i is a positive integer) (In the portions (A) and (B) of Fig. 2, i is any one of 1 to 3, and in the portion (C) thereof, i is any one of 10, 20, 30, and 40) within a circuit to be simulated, for example, a net N1 in the portion (A) of Fig. 2 is selected (step S200). An identification number marking a net concerned is assigned to the net Ni, for example, net N1. That is to say, an identification number a1 is assigned to the net N1 (step S210).

At step S220 shown in Fig. 1A, circuit elements interconnected within the net Ni and exhibiting the same

characteristics (identical circuit elements) are inspected. What is referred to as identical circuit elements are circuit elements exhibiting the same characteristics such as NMOS transistors or p-type MOS (PMOS) transistors that are active circuit elements to be operated with power supplied from a source power supply VDD and drain power supply VSS, capacitors that are passive circuit elements, resistors, and diodes. That is to say, the identical circuit elements are circuit elements exhibiting mutually equivalent operational characteristics. For example, an NMOS transistor Q1 and NMOS transistor Q2 shown in the portion (A) of Fig. 2 are regarded as identical circuit elements.

If a plurality of identical circuit elements are detected at step S230, control is passed to step S240. Otherwise, control is passed to step S290. At step S240, the same identification number is assigned to the identical circuit elements detected at step S220. For example, an identification number b1 is assigned to both the NMOS transistor Q1 and NMOS transistor Q2 (step S240).

As shown in Fig. 1B, it is checked if corresponding terminals of the thus detected identical circuit elements exhibit the same characteristics (step S245). For example, in the portion (A) of Fig. 2, it is checked if the electrical conditions for connection of the source, drain, and bulk resistor of the NMOS transistor Q1 are the same as those of the source, drain, and bulk resistor of the NMOS transistor Q2 (step 250).

Further, in Fig. 1B, if the thus inspected corresponding terminals exhibit the same characteristics, control is passed to step S260. Otherwise, control is passed to step S280.

At step S260 shown in Fig. 1B, m (m is a positive integer equal to or larger than 2) circuit elements and terminals thereof exhibiting the same characteristics are integrated into one circuit element

and terminals thereof. For example, the circuit elements shown in the portion (A) of Fig. 2 are integrated into the circuit element shown in the portion (B) thereof. Converting a circuit composed of a plurality of circuit elements and a plurality of terminals into a circuit having one simple circuit element and terminals is referred to as circuit compression.

For compressing the circuit shown in the portion (A) of Fig. 2 into the circuit shown in the portion (B) thereof, the characteristics of an NMOS transistor Q1' must be determined so that a current flowing through the terminals of the NMOS transistor Q1' (refer to the portion (B) of Fig. 2) will be twice as large as a current flowing through the terminals of the NMOS transistor Q1 that has not been integrated (refer to the portion (A) of Fig. 2). In other words, the parameters of the circuit element are determined so that the gate capacitance and drain current of the NMOS transistor Q1' will be twice as large as those of the NMOS transistor Q1.

At a result of inspecting terminals to which the same identification number has been assigned, if it is recognized at step S280 that the terminals are not identical to each other, the identification number is released (for example, the identification number b1 assigned to the NMOS transistors Q1 and Q2 shown in the portion (A) of Fig. 2 is released). The control flow is then returned to step S220. Regarding circuit elements and terminals having identification numbers assigned thereto, circuit elements and terminals having the same identification number can be judged to exhibit the same characteristics. Repetition of a sequence for judging if circuit elements exhibit the same characteristics can be avoided.

Regarding an NMOS transistor Q10 and NMOS transistor Q20 in the logic circuit shown in the portion (C) of Fig. 2 which have been judged as identical circuit

elements according to the same procedure adopted to inspect the circuit elements shown in the portion (A) of Fig. 2 and to which the same identification number b10 has been assigned, the drains thereof are connected to the nets N20, and the bulk resistors thereof are connected to the nets N30. However, the source of the NMOS transistor Q10 is connected to the net N30, while the source of the NMOS transistor Q10 is connected to the net N40. The sources of the NMOS transistor Q10 and NMOS transistor Q20 must be inspected in order to check if they exhibit the same characteristics, even though the same identification number t1 has already been assigned to the sources.

For inspecting the sources of the NMOS transistor Q10 and NMOS transistor Q20 to check if they exhibit the same characteristics, the circuit elements connected to the sources that are corresponding terminals are inspected in order to check if they exhibit the same characteristics. In the case of the portion (C) of Fig. 2, the source of the NMOS transistor Q10 is connected to a source power supply VSS, while the source of the NMOS transistor Q20 is connected to the drain of the NMOS transistor Q30. It is therefore judged that the source of the NMOS transistor Q10 and the source of the NMOS transistor Q20 do not exhibit the same characteristics. In this case, the same identification number t1 assigned to the sources is released at step S280.

According to the circuit simulation method of the related art described in conjunction with Figs. 1A, 1B and 2, circuit simulation is carried out by compressing a circuit that includes circuit elements that have been verified to exhibit the same characteristics as a result of inspecting the circuit elements to check if they exhibit the same characteristics (that is, if the operational characteristics thereof are equivalent to each other) on the basis of the connectional relationship of an input terminal of the circuit to be simulated, the

configuration of the circuit to be simulated, and the operational characteristics of the plurality of corresponding circuit elements.

However, according to the circuit simulation method of the related art, as described in conjunction with Figs. 1A, 1B and 2, when the operations of a circuit to be simulated such as a MOS LSI circuit are inspected, a plurality of circuit elements that have been judged to exhibit the same characteristics are finally inspected for equivalence in operational characteristics merely by inspecting circuit elements connected to corresponding terminals of the plurality of circuit elements to see if they exhibit the same characteristics.

As mentioned above, according to the circuit simulation method of the related art, only circuit elements located in a limited area within a circuit can be inspected in order to see if they exhibit the same characteristics. It is difficult to distinguish all circuit elements exhibiting equivalent operational characteristics in a circuit to be simulated. The circuit is therefore not compressed effectively.

The total number of circuit elements increases with an increase in scale of a circuit to be simulated. The time required for simulation therefore increases. This causes the problem in that it is hard to achieve circuit simulation at high speed.

SUMMARY OF THE INVENTION

The present invention attempts to solve the foregoing problems. An object of the present invention is to provide a method and apparatus for carrying out circuit simulation in which, when especially a large-scale circuit such as a MOS LSI circuit is selected as an object of simulation, the time required for simulation can be shortened drastically, and therefore high-speed simulation can be realized.

For solving the aforesaid problem, a method for carrying out circuit simulation in accordance with the

present invention is such that: a plurality of partial circuits to be inspected for equivalence in order to check if they exhibit equivalent operational characteristics are extracted from a circuit that is an object of circuit simulation; the intensity of the influence of an external terminal of the circuit is assessed, by tracing paths linking the external terminal and given terminals of the plurality of partial circuits; based on the configurations of the plurality of partial circuits, the connectional relationships of at least ones of the corresponding input terminals and the output terminals of the plurality of partial circuits, the operational characteristics of corresponding component elements of the plurality of partial circuits, and the intensity of the influence of the external terminal, the plurality of partial circuits are inspected for equivalence in order to detect partial circuits exhibiting equivalent operational characteristics; and after the circuit is compressed by integrating the partial circuits exhibiting the equivalent operational characteristics into one circuit, circuit simulation is carried out.

Preferably, in a method for carrying out circuit simulation in accordance with the present invention, when the circuit is a MOS circuit including a plurality of MOS semiconductor devices, the frequency of shifting from the source or drain of a MOS semiconductor device to the gate thereof while tracing a path linking the external terminal and a given terminal of each of the plurality of partial circuits is assessed as the intensity of the influence of the external terminal.

More preferably, in a method for carrying out circuit simulation in accordance with the present invention, when the connectional relationships of at least ones of the corresponding input terminals and output terminals of the plurality of partial circuits to be inspected for equivalence are judged to be mutually

inconsistent, a plurality of other partial circuits connected to at least ones of the input terminals and output terminals are inspected for quasi-equivalence. When the plurality of other partial circuits are judged as quasi-equivalent circuits, the plurality of partial circuits to be inspected for equivalence are regarded to exhibit equivalent operational characteristics.

More preferably, in a method for carrying out circuit simulation in accordance with the present invention, when a plurality of partial circuits are inspected for equivalence, a unique element having no counterpart within the circuit is detected. If a terminal that has not been judged as a unique terminal having no counterpart is included in terminals connected to the unique element, the terminal is newly judged as a unique terminal. The plurality of partial circuits connected to the newly judged unique terminal are inspected for equivalence.

An apparatus for carrying out circuit simulation in accordance with the present invention includes a circuit extracting unit for extracting a plurality of partial circuits, which will be inspected for equivalence in order to check if they exhibit equivalent operational characteristics, from a circuit that is an object of circuit simulation; a storage unit for holding data concerning the configurations of the plurality of partial circuits, the connectional relationships of at least ones of the corresponding input terminals and output terminals of the plurality of partial circuits, and the operational characteristics of corresponding component elements of the plurality of partial circuits; an assessing unit for assessing the intensity of influence of an external terminal of the circuit, by tracing paths linking the external terminal and given terminals of the plurality of partial circuits; and a circuit-equivalence inspecting circuit for detecting partial circuits exhibiting equivalent operational characteristics by inspecting the

plurality of partial circuits for equivalence, on the basis of the results of assessment concerning the intensity of the influence of the external terminal provided by the assessing unit and the data held by the storage unit. Herein, after the circuit is compressed by integrating the partial circuits exhibiting the equivalent operational characteristics into one circuit, circuit simulation is carried out.

Preferably, in an apparatus for carrying out circuit simulation in accordance with the present invention, when the circuit is a MOS circuit including a plurality of MOS semiconductor devices, the assessing unit assesses, as the intensity of the influence of the external terminal, the frequency of shifting from the source or drain of a MOS semiconductor device to the gate thereof while tracing a path linking the external terminal to a given terminal of each of the plurality of partial circuits.

Preferably, an apparatus for carrying out circuit simulation in accordance with the present invention further comprises a connected-circuit quasi-equivalence inspecting unit for, when the connectional relationships of at least ones of the corresponding input terminals and output terminals of the plurality of partial circuits to be inspected for equivalence are judged to be mutually inconsistent, inspecting for quasi-equivalence a plurality of other partial circuits connected to at least ones of the input terminals and output terminals. When the connected-circuit quasi-equivalence inspecting unit judges that the plurality of other partial circuits are quasi-equivalent circuits, the plurality of partial circuits to be inspected for equivalence are regarded to exhibit equivalent operational characteristics.

More preferably, in an apparatus for carrying out circuit simulation in accordance with the present invention, when the circuit-equivalence inspecting circuit inspects a plurality of partial circuits for equivalence, it detects a unique element having no

counterpart within the circuit. When a terminal that has not been judged as a unique terminal having no counterpart is included in terminals connected to the unique element, the terminal is newly judged as a unique terminal. The plurality of partial circuits connected to the newly judged unique terminal are inspected for equivalence.

According to a method or apparatus for carrying out circuit simulation in accordance with the present invention, the intensity of the influence to be assessed as the frequency of shifting from the source or drain of a MOS semiconductor device to the gate thereof in the course of tracing a path linking an external terminal of extracted partial circuits to an object terminal is taken into account in order to inspect the partial circuits for equivalence. Integrating a plurality of partial circuits into one circuit, which cannot be achieved according to a known technique, can be achieved readily. As a result, a circuit to be simulated can be compressed more effectively. Consequently, the scale of the circuit to be simulated gets smaller. Eventually, circuit simulation can be executed at relatively high speed.

BRIEF DESCRIPTION OF THE DRAWINGS

The above object and features of the present invention will be more apparent from the following description of the preferred embodiments with reference to the accompanying drawings, wherein:

Figs. 1A and 1B are flowcharts each for explaining an example of a circuit simulation method in accordance with the related art;

Fig. 2 is a circuit diagram showing a typical example of a circuit to be simulated which will be compressed according to the circuit simulation method described in Fig. 1;

Fig. 3 is a flowchart for explaining a method for carrying out circuit simulation in accordance with a fundamental embodiment of the present invention based on

the principle of the present invention;

Fig. 4 is a block diagram showing the configuration of an apparatus for carrying out circuit simulation in accordance with the fundamental embodiment of the present invention based on the principle of the present invention;

Fig. 5 is a flowchart describing an algorithm, according to which two partial circuits are inspected for equivalence in operation, employed in a method for carrying out circuit simulation in accordance with a preferred embodiment of the present invention;

Fig. 6 is a flowchart describing an algorithm, according to which two partial circuits are inspected for quasi-equivalent in operation, employed in the method for carrying out circuit simulation in accordance with the preferred embodiment of the present invention;

Fig. 7 is a block diagram showing the configuration of an apparatus for carrying out circuit simulation in accordance with the preferred embodiment of the present invention;

Fig. 8 is a circuit diagram for explaining the intensity of influence of an external terminal upon terminals;

Fig. 9 is a circuit diagram showing the first example of a circuit whose partial circuits are judged as equivalent circuits according to the algorithm described in Fig. 5;

Fig. 10 is a circuit diagram showing an example of a circuit whose partial circuits are not judged as equivalent circuits according to the algorithm described in Fig. 5;

Fig. 11 is a circuit diagram showing the second example of a circuit whose partial circuits are judged as equivalent circuits according to the algorithm described in Fig. 5;

Fig. 12 is a circuit diagram showing an example of a circuit whose partial circuits are judged as

quasi-equivalent circuits according to the algorithm described in Fig. 6;

Fig. 13 is a circuit diagram showing the configuration of a compressed form of the circuit shown in Fig. 11; and

Fig. 14 is a flowchart describing an algorithm, according to which an element and terminal are inspected for uniqueness, employed in the method for carrying out circuit simulation in accordance with the preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to the appended drawings of Figs. 3 to 14, the fundamental embodiment and preferred embodiment of the present invention will be described.

Fig. 3 is a flowchart for explaining a method for carrying out circuit simulation in accordance with the fundamental embodiment of the present invention based on the principle of the present invention.

According to the method for carrying out circuit simulation in accordance with the fundamental embodiment of the present invention based on the principle of the present invention, a plurality of partial circuits to be inspected for equivalence in order to check if they exhibit equivalent operational characteristics are extracted from a circuit that is an object of circuit simulation (that is, a circuit to be simulated) (step S1). The intensity of the influence of an external terminal of the circuit to be simulated is assessed by tracing paths linking the external terminal and given terminals of the plurality of partial circuits (step S2). Based on the configurations of the plurality of partial circuits, the connectional relationships of at least ones of the corresponding input terminals and output terminals of the plurality of partial circuits, the operational characteristics of corresponding component elements (that is, circuit elements) of the plurality of partial circuits, and the intensity of the influence of the

external terminal, the plurality of partial circuits are inspected for equivalence in order to detect partial circuits exhibiting equivalent operational characteristics (step S3). After the circuit to be simulated is compressed by integrating the partial circuits exhibiting the equivalent operational characteristics into one circuit, circuit simulation is carried out (step S4).

Preferably, according to a method for carrying out circuit simulation in accordance with the fundamental embodiment of the present invention, when the circuit is a MOS circuit including a plurality of MOS semiconductor devices, the frequency of shifting from the source or drain of a MOS semiconductor device toward the gate thereof while tracing a path linking the external terminal and a given terminal of each of the plurality of partial circuits is assessed as the intensity of influence of the external terminal.

More preferably, according to a method for carrying out circuit simulation in accordance with the fundamental embodiment of the present invention, when the connectional relationships of at least ones of the corresponding input terminals and output terminals of the plurality of partial circuits to be inspected for equivalence are judged to be mutually inconsistent, a plurality of other partial circuits connected to at least ones of the input terminals and output terminals are inspected for quasi-equivalence. When the plurality of other partial circuits are judged as quasi-equivalent circuits, the plurality of partial circuits to be inspected for equivalence are regarded to exhibit equivalent operational characteristics.

More preferably, according to a method for carrying out circuit simulation in accordance with the fundamental embodiment of the present invention, when the plurality of partial circuits are inspected for equivalence, a unique element having no counterpart within the circuit

is detected. When a terminal that has not been judged as a unique terminal having no counterpart is included in terminals connected to the unique element, the terminal is newly judged as a unique terminal. A plurality of partial circuits connected to the newly judged unique terminal are inspected for equivalence.

Fig. 4 is a block diagram showing the configuration of an apparatus for carrying out circuit simulation in accordance with the fundamental embodiment of the present invention based on the principle of the present invention. For brevity's sake, the configuration of an apparatus for carrying out circuit simulation including a circuit simulator is shown schematically.

The apparatus for carrying out circuit simulation in accordance with the present invention comprises: as shown in the block diagram of Fig. 4, a circuit extracting unit 1 for extracting a plurality of partial circuits, which will be inspected for equivalence in order to check if they exhibit equivalent operational characteristics, from a circuit that is an object of circuit simulation (that is, a circuit to be simulated); and a storage unit 5 for holding data concerning the configurations of the plurality of partial circuits, the connectional relationships of at least ones of the corresponding input terminals and output terminals of the plurality of partial circuits, and the operational characteristics of corresponding component elements (that is, circuit elements) of the plurality of partial circuits. The storage unit 5 has the ability to hold a prescribed value concerning quasi-equivalent circuits and the results of equivalence inspection.

Furthermore, the apparatus for carrying out circuit simulation in accordance with the fundamental embodiment of the present invention shown in Fig. 4 comprises: an assessing unit for assessing the intensity of influence of an external terminal of the circuit by tracing paths linking the external terminal and given terminals of the

plurality of partial circuits; and a circuit-equivalence inspecting circuit 2 for detecting partial circuits exhibiting equivalent operational characteristics by inspecting the plurality of partial circuits for equivalence on the basis of the results of assessment concerning the intensities of influence of the external terminal provided by the assessing unit and the data held by the storage unit 5. After the circuit is compressed by integrating the partial circuits exhibiting the equivalent operational characteristics into one circuit, circuit simulation is carried out.

Preferably, the assessing unit is realized by a control unit 6 including a CPU and connected to the storage unit 5, circuit extracting unit 1, and circuit-equivalence inspecting circuit 2. The control unit 6 also controls various data streams and judges from the results of equivalence inspection performed by the circuit-equivalence inspecting circuit 2 whether or not partial circuits exhibit equivalent operational characteristics.

Furthermore, the apparatus for carrying out circuit simulation in accordance with the fundamental embodiment of the present invention shown in Fig. 4 comprises a data input unit 4 connected to the control unit 6. The data input unit 4 has the ability to input data concerning the configurations of a plurality of partial circuits, the connectional relationships of at least ones of the corresponding input terminals and output terminals of the plurality of partial circuits, the operational characteristics of corresponding component elements of the plurality of partial circuits, and a prescribed value concerning quasi-equivalent circuits to the control unit 6. Moreover, the apparatus for carrying out circuit simulation shown in Fig. 4 comprises an output display unit 7 for displaying the results of inspecting the plurality of partial circuits for equivalence.

Preferably, when the circuit is a MOS circuit

including a plurality of MOS semiconductor devices, the assessing unit assesses, as the intensity of the influence of the external terminal, the frequency of shifting from the source or drain of a MOS semiconductor device toward the gate thereof while tracing a path linking an external terminal and a given terminal of each of the plurality of partial circuits.

Furthermore, preferably, the apparatus for carrying out circuit simulation in accordance with the fundamental embodiment of the present invention shown in Fig. 4 comprises a connected-circuit quasi-equivalence inspecting unit 3 connected to the control unit 6. When the circuit-equivalence inspecting circuit 2 judges that the connectional relationships of at least ones of corresponding input terminals and output terminals of the plurality of partial circuits to be inspected for equivalence are mutually inconsistent, the connected-circuit quasi-equivalence inspecting unit 3 inspects a plurality of other partial circuits connected to at least ones of the input terminals and output terminals for quasi-equivalence. In this case, when the connected-circuit quasi-equivalence inspecting unit 3 judges that the plurality of other partial circuits are quasi-equivalent circuits, the plurality of partial circuits to be inspected for equivalence are regarded to exhibit equivalent operational characteristics.

Furthermore, preferably, in the apparatus for carrying out circuit simulation in accordance with the fundamental embodiment of the present invention shown in Fig. 4, when the circuit-equivalence inspecting circuit 2 inspects a plurality of partial circuits for equivalence, it detects a unique element having no counterpart within the circuit. When a terminal that has not been judged as a unique terminal having no counterpart is included in terminals connected to the unique element, the terminal is newly judged as a unique terminal. A plurality of partial circuits connected to the newly judged unique

terminal are inspected for equivalence.

For carrying out simulation using the apparatus for carrying out circuit simulation, first, partial circuits exhibiting the same operational characteristics are distinguished in a circuit to be simulated such as a MOS LSI circuit. For distinguishing partial circuits, the intensity of the influence of an external terminal of the extracted partial circuits upon the extracted partial circuits is taken into account. The intensity of the influence of the external terminal is assessed as the frequency of shifting from the source or drain of a MOS semiconductor device (for example, MOS transistor) to the gate thereof in the course of tracing a path linking the external terminals and an object terminal. When a plurality of partial circuits are inspected for equivalence, even if the connected states of corresponding external terminals of two partial circuits are mutually inconsistent, as long as the intensities of currents flowing from the external terminals placed in the inconsistent connected states are equal to or larger than a designated value, it is regarded that the influence of the external terminals is negligible. Consequently, the partial circuits are judged to exhibit equivalent operational characteristics.

For inspecting partial circuits for equivalence through comparison, the uniqueness of an element and terminal is detected, or in other words, it is detected that an element and terminal has no counterpart, that is, that one partial circuit has no counterpart capable of being compressed. In short, a partial circuit including an element that is confirmed to be unique has no counterpart exhibiting equivalent operational characteristics. Consequently, when partial circuits are inspected for equivalence through comparison, partial circuits other than a partial circuit including an element that is confirmed to be unique should merely be inspected.

When the apparatus for carrying out circuit simulation shown in Fig. 4 is used to carry out circuit simulation, partial circuits exhibiting equivalent operational characteristics, which are detected by the circuit-equivalence inspecting circuit 2, are integrated into one circuit and analyzed for operational characteristics. For analyzing partial circuits for operational characteristics, partial circuits integrated into one circuit are, in principle, analyzed by carrying out the same calculation as the one used to analyze partial circuits that are not integrated. The processing described below is performed on circuit elements located on the border between partial circuits to be integrated.

When circuit elements of partial circuits to be integrated are connected to the same terminal, a value indicating an operational characteristic of the terminal is multiplied by the number of partial circuits to be integrated. When circuit elements of partial circuits to be integrated are connected to different terminals, the partial circuits integrated are analyzed while being regarded to be connected to either of the destinations to which they were originally connected. The results of analysis are handled in relation to the different terminals. Thus, the operational characteristics of the partial circuits are analyzed.

According to the method or apparatus for carrying out circuit simulation in accordance with the fundamental embodiment of the present invention, the influence of an external terminal of extracted partial circuits to be assessed as the frequency of shifting from the source or drain of a MOS semiconductor device to the gate thereof in the course of tracing a path linking the external terminal to an object terminal is taken into consideration. The partial circuits are then inspected for equivalence. Consequently, integrating a plurality of partial circuits into one circuit readily, which cannot be achieved according to a known technique, can be

achieved readily. As a result, a circuit to be simulated can be compressed more effectively. The scale of the circuit to be simulated can be reduced sufficiently. Thus, simulation of a circuit can be carried out at a relatively high speed.

Referring to Figs. 5 to 14, a preferred embodiment of the present invention will be described. The same reference numerals will be assigned to components identical to those described previously.

Fig. 5 is a flowchart describing an algorithm, according to which two partial circuits are inspected for equivalence in operation, employed in a method for carrying out circuit simulation in accordance with a preferred embodiment of the present invention.

Fig. 5 describes an example of an algorithm used to inspect two partial circuits for equivalence. First, partial circuits to be inspected for equivalence through comparison are extracted from a circuit that is an object of circuit simulation (step S11). Every time partial circuits to be inspected through comparison are extracted, the processing of step 11 is repeated. First, the configurations of the two partial circuits (that is, what kinds of circuit elements are interconnected) are compared with each other (step S12). If the configurations are even partly inconsistent with each other, it is judged that the partial circuits have no equivalence between them (step S17). By contrast, when the configurations of two partial circuits are perfectly consistent with each other, control is passed to step S13. At step S13, the configurations of the two partial circuits are compared with each other, the operational characteristics of the corresponding circuit elements are compared with each other. If the operational characteristics of the circuit elements are mutually inconsistent, the operational characteristics of the partial circuits including the circuit elements are judged not to be equivalent to each other (step S17).

If all pairs of corresponding circuit elements have the same operational characteristics, at least ones of the input terminals and output terminals (hereinafter abbreviated to input or output terminals) of the partial circuits including the circuit elements are compared with each other (step S14). Step S14 is a step of judging whether or not corresponding input or output terminals are identical to each other. If corresponding input or output terminals are mutually identical, it is judged that the operational characteristics of the partial circuits being compared with each other are equivalent to each other (step S16).

In contrast, if mutually-different input or output terminals are present, it is judged whether or not partial circuits connected to the input or output terminals (however, partial circuits inspected for equivalence through comparison are excluded) are quasi-equivalent circuits, that is, the partial circuits connected to the input or output terminals are inspected for quasi-equivalence (step S15). When it is judged that partial circuits connected to all mutually-different input or output terminals are quasi-equivalent circuits, the partial circuits being inspected through comparison are judged to have equivalence between them (step S16). Otherwise, it is judged that the partial circuits have no equivalence between them (step S17).

Fig. 6 is a flowchart describing an algorithm, according to which two partial circuits are inspected for quasi-equivalence, employed in the method for carrying out circuit simulation in accordance with the preferred embodiment of the present invention.

In Fig. 6, for inspecting two partial circuits for quasi-equivalence in operation, first, the configurations of partial circuits to be compared with each other for quasi-equivalence are checked (step S21). As a result, if the configurations of the partial circuits are even partly mutually different, it is judged that the partial

circuits are not quasi-equivalent to each other (step S24). If the configurations of the partial circuits are identical to each other, corresponding circuit elements are inspected in order to check if the operational characteristics thereof are identical to each other (step S22). If even one circuit element exhibits different operational characteristics, the partial circuits are judged not to be quasi-equivalent to each other (step S24). In contrast, as a result of comparing the operational characteristics of all circuit elements, if the operational characteristics are judged to be mutually identical, the control flow is passed to step S23. At step S23, the intensity of influence of an external terminal of circuits being inspected for quasi-equivalence upon input or output terminals that are determinants of judgment of quasi-equivalence are calculated (step S23). If the intensity of influence are equal to or larger than a prescribed value, it is judged that the two partial circuits have quasi-equivalence between them (step S25). Otherwise, it is judged that the two partial circuits have no quasi-equivalence between them (step S24).

Fig. 7 is a block diagram showing the configuration of an apparatus for carrying out circuit simulation in accordance with the preferred embodiment of the present invention. A computer system including a computer and external storage unit is shown as a practical example of the apparatus for carrying out circuit simulation based on the principle of the present invention shown in Fig. 4.

In the preferred embodiment shown in Fig. 7, the control unit 6, circuit extracting unit 1, circuit-equivalence inspecting circuit 2, connected-circuit quasi-equivalence inspecting unit 3, and assessing unit for assessing the intensity of influence of an external terminal of a circuit to be simulated are realized with a computer 60 including a

CPU.

Referring to Fig. 7, the storage unit 5 shown in Fig. 3 is realized with an external storage unit 50 such as a magneto-optical disk unit or magnetic disk unit. The external storage unit 50 holds circuit data 51 concerning the configurations of a plurality of partial circuits, the connectional relationships of corresponding input or output terminals of the plurality of partial circuits, and the operational characteristics of corresponding circuit elements of the plurality of partial circuits, a prescribed value 52 concerning quasi-equivalent circuits such as a value indicating the intensity of the influence of an external terminal, and data concerning inspection result 53 which indicates the presence or absence of equivalence or quasi-equivalence.

In Fig. 7, there is shown a data input unit 40 as an example of the data input unit 4 shown in Fig. 3. The data input unit 40 has the ability to input data concerning the configurations of a plurality of partial circuits, the connectional relationships of corresponding input or output terminals of the plurality of partial circuits, and the operational characteristics of corresponding component elements of the plurality of partial circuits, and a prescribed value concerning quasi-equivalent circuits into the computer 60.

In Fig. 7, there are shown a display unit 70 for displaying the results of inspecting a plurality of partial circuits for equivalence in a screen as a substitute for the output display unit 7 shown in Fig. 3, and a printer unit 72 for printing and displaying the results of inspecting a plurality of partial circuits for equivalence.

In the embodiment, the CPU in the computer 60 operates at high speed so as to inspect partial circuits for equivalence or quasi-equivalence in operation according to the algorithm described in Fig. 5 or 6.

Fig. 8 is a circuit diagram for explaining the

intensity of the influence of an external terminal upon terminals. Herein, a logic circuit composed of a plurality of PMOS transistors and NMOS transistors exhibiting the same operational characteristics is shown as an example of a circuit that is an object of circuit simulation.

In Fig. 8, there are shown terminals A to H. Also shown are PMOS transistors Ta, Tb, Tf, Th, Ti, and Tk, and NMOS transistors Tc, Td, Te, Tg, Tj, and Tl. Filled dots in Fig. 8 indicate nodes joining different circuit elements.

In Fig. 8, the intensities of the influence of the external terminal A of the circuit to be simulated upon the terminals are indicated. Specifically, numerical values in parentheses appended to the terminal names in Fig. 8 indicate the intensity of influence upon the terminals. For example, when it comes to the terminal E, a path linking the terminal A serving as an external terminal and the terminal E is A to Tb to C to Th to E. Along the path, the frequency of shifting from the source or drain of a MOS transistor to the gate thereof is two. The intensity of influence upon the terminal E is therefore 2. If there are a plurality of paths, the smallest intensity of influence is defined as the intensity of influence upon a terminal concerned.

Fig. 9 is a circuit diagram showing the first example of a circuit whose partial circuits are judged as equivalent circuits according to the algorithm described in Fig. 5.

Herein, a logic circuit composed of four PMOS transistors T1, T3, T5, and T6, and four NMOS transistors T2, T4, T7, and T8 is shown as an example of a circuit that is an object of circuit simulation. Even in this case, the PMOS transistors and NMOS transistors all exhibit the same operational characteristics. Moreover, two signals to be input to a first partial circuit 11 and second partial circuit 12 through an input terminal have

the same waveform.

Fig. 9 shows an example of a circuit including the first partial circuit 11 and second partial circuit 12 which are judged to exhibit equivalent operational characteristics. Specifically, when corresponding input or output terminals of the two partial circuits 11 and 12 are compared with each other, it is recognized that the corresponding input or output terminals are identical to each other. Finally, the operational characteristics of the two partial circuits 11 and 12 are judged to be equivalent to each other.

Fig. 10 is a circuit diagram showing an example of a circuit whose partial circuits are not judged as equivalent circuits according to the algorithm described in Fig. 5.

Herein, a logic circuit composed of four PMOS transistors T11, T13, T15, and T16 and four NMOS transistors T12, T14, T17, and T18 is shown as an example of a circuit that is an object of circuit simulation. Even in this case, the PMOS transistors and NMOS transistors all exhibit the same operational characteristics. Moreover, two signals to be input to a first partial circuit 21 and second partial circuit 22 through an input terminal have the same waveform.

Fig. 10 shows an example of a circuit whose first partial circuit 21 and second partial circuit 22 are judged not to exhibit mutually equivalent operational characteristics. Specifically, when corresponding input or output terminals of the two partial circuits 21 and 22 are compared with each other, it is recognized that the output terminals of the two partial circuits 21 and 22 are connected to different NMOS transistors T17 and T18. It is therefore judged that the operational characteristics of the two partial circuits 21 and 22 are not equivalent.

Fig. 11 is a circuit diagram showing a second example of a circuit whose partial circuits are judged as

equivalent circuits according to the algorithm described in Fig. 5.

Herein, a logic circuit composed of ten PMOS transistors and ten NMOS transistors (T20 to T39) is shown as an example of a circuit that is an object of circuit simulation. Even in this case, the PMOS transistors and NMOS transistors all exhibit the same operational characteristics. Furthermore, two signals to be input to a first partial circuit 31 and second partial circuit 32 have the same waveform.

Fig. 11 shows an example of a circuit whose first partial circuit 31 and second partial circuit 32 exhibit mutually equivalent operational characteristics. Specifically, when corresponding input or output terminals of the two partial circuits 31 and 32 are compared with each other, it is recognized that the corresponding input or output terminals are identical to each other. It is therefore judged that the operational characteristics of the two partial circuits 31 and 32 are equivalent to each other.

Fig. 12 is a circuit diagram showing an example of a circuit whose partial circuits are judged as quasi-equivalent circuits according to the algorithm described in Fig. 6.

Herein, a logic circuit composed of ten PMOS transistors and ten NMOS transistors (T40 to T59) is, like the one in Fig. 11, shown as an example of a circuit that is an object of circuit simulation. Even in this case, the PMOS transistors and NMOS transistors all exhibit the same operational characteristics. Moreover, two signals to be placed on two lines through an input terminal have the same waveform.

In the circuit to be simulated shown in Fig. 12, a prescribed value indicating the intensity of the influence upon a quasi-equivalent circuit is set to 2. Fig. 12 shows an example of a circuit whose first partial circuit 33 and second partial circuit 34 are judged as

quasi-equivalent circuits. In the example shown in Fig. 12, the output destination through a terminal A of one equivalent circuit composed of PMOS transistors T40, T44, and T48 and NMOS transistors T41, T45, and T49 is different from the output destination through a terminal B of the other equivalent circuit composed of PMOS transistors T42, T46, and T50 and NMOS transistors T43, T47, and T51. According to the algorithm described in Fig. 6, it is recognized that the configurations of the output destinations that are partial circuits (that is, the first partial circuit 33 and second partial circuit 34) and the operational characteristics of corresponding circuit elements are mutually identical. The mutually different connectional relationships of corresponding input or output terminals of the first partial circuit 33 and second partial circuit 34 are connections to NMOS transistors T58 and T59. The intensity of the influence of the NMOS transistors T58 and T59 upon the terminals A and B are 2 that is equal to the prescribed value. Consequently, the first partial circuit 33 and second partial circuit 34 are judged as quasi-equivalent circuits. Eventually, it is judged that the operational characteristics of partial circuits in Fig. 12 corresponding to the first partial circuit 31 and second partial circuit 32 shown in Fig. 11 are equivalent to each other.

Fig. 13 is a circuit diagram showing the configuration of a compressed form of the circuit shown in Fig. 11.

Herein, a compressed partial circuit is composed of three PMOS transistors Pa, Pc, and Pe and three NMOS transistors Pb, Pd, and Pf. That is to say, the numbers of circuit elements of the first partial circuit 31 and first partial circuit 32 shown in Fig. 9 are compressed to a half. Aside from the above MOS transistors, the circuit shown in Fig. 13 includes four PMOS transistors and four NMOS transistors (T62 to T69).

Circuit simulation is performed on a compressed circuit similar to the one shown in Fig. 13. In this case, it should be noted that compressed partial circuits are handled differently from a normal circuit. When the partial circuits are analyzed in relation to a terminal C, calculation is carried out with a current flowing from the PMOS transistor Pa doubled (comparable to the number of circuit elements compressed). The same applies to a terminal D. When the partial circuits are analyzed in relation to a terminal G, the connection between the terminal G and a terminal G', which is drawn with a dashed line in Fig. 13, is regarded as not being made. When the partial circuits are analyzed in relation to a terminal H, the terminal G' is handled as if it were the terminal G. Thus, the compressed circuit is simulated.

Fig. 14 is a flowchart describing an algorithm, according to which a circuit element and terminal are inspected for uniqueness, employed in the method for carrying out circuit simulation in accordance with a preferred embodiment of the present invention. Herein, circuit elements constituting a circuit to be simulated shall be referred to simply as elements.

According to the algorithm described in Fig. 14, first, a unique element is detected (step S31). For example, a power supply that operates uniquely is a unique element. If there is a counterpart that operates in the same manner as the power supply, these power supplies are integrated into one power supply. The power supply is then handled as a unique element. When a unique element is detected, terminals connected to the detected element are inspected to see if the terminals have been judged to be unique (step S32). If there is a terminal that has not been judged to be unique, the terminal is newly judged as a unique terminal (step S33).

When all the terminals connected to all elements that have been judged to be unique are judged to be unique, the processing is terminated (step 37). In

contrast, as far as a terminal newly judged to be unique is concerned, partial circuits connected to the terminal are inspected for equivalence in operational characteristics (step S34). If the operational characteristics of the partial circuits are judged to be equivalent to each other, compression is carried out in order to integrate the partial circuits into one circuit (step S35). After the compression is completed, elements connected to the terminal that is judged to be unique are newly judged to be unique (step S36). By repeating this sequence, the uniqueness of an element and terminal is judged and a circuit is compressed.

As described so far, according to the fundamental embodiment and preferred embodiment of the present invention, first, the intensity of influence of an external terminal of partial circuits extracted from a circuit to be simulated is assessed by tracing paths linking the external terminal and object terminals. The partial circuits are thus inspected for equivalence. Integrating a plurality of partial circuits into one circuit, which cannot be achieved according to a known technique, can be achieved readily. The circuit to be simulated can be compressed effectively and reduced sufficiently in scale. Consequently, circuit simulation can be carried out at a relatively high speed.

According to the fundamental embodiment and preferred embodiment of the present invention, second, the frequency of shifting from the source or drain of a MOS semiconductor device to the gate thereof in the course of tracing a path linking an external terminal and an object terminal is assessed as the intensity of influence of the external terminal. Partial circuits can therefore be inspected for equivalence with higher precision than they can be inspected according to a related art. Consequently, a large-scale circuit such as a MOS LSI circuit can be compressed effectively. The time required for simulation of a MOS LSI circuit or the

like is shortened drastically. Eventually, circuit simulation can be carried out at high speed.

According to the fundamental embodiment and preferred embodiment of the present invention, third, when the connectional relationships of corresponding input or output terminals of a plurality of partial circuits to be inspected for equivalence are judged to be mutually inconsistent, a plurality of other partial circuits connected to the input or output terminals are inspected for quasi-equivalence. Based on the results of quasi-equivalence inspection, the partial circuits to be inspected for equivalence can be inspected for equivalence quickly and accurately. Consequently, the time required for compressing a circuit to be simulated can be shortened drastically.

According to the fundamental embodiment and preferred embodiment of the present invention, fourth, when partial circuits are inspected for equivalence, a unique element having no counterpart within a circuit to be simulated is detected, and a unique terminal is distinguished from terminals connected to the unique element. Partial circuits other than a partial circuit including a circuit element that is recognized as a unique element can be extracted readily as partial circuits which need to be inspected for equivalence.

CLAIMS

1. A method for carrying out circuit simulation, including the steps of:

extracting a plurality of partial circuits to be inspected for equivalence in order to check if they exhibit equivalent operational characteristics, from a circuit that is an object of circuit simulation;

assessing the intensity of influence of an external circuit of said circuit, by tracing paths linking said external terminal and given terminals of said plurality of partial circuits;

inspecting said plurality of partial circuits for equivalence in order to detect partial circuits exhibiting equivalent operational characteristics, based on the configurations of said plurality of partial circuits, the connectional relationships of at least ones of the corresponding input terminals and output terminals of said plurality of partial circuits, the operational characteristics of corresponding component elements of said plurality of partial circuits, and the intensity of the influence of said external terminal; and

carrying out circuit simulation after said circuit is compressed by integrating said partial circuits exhibiting equivalent operational characteristics into one circuit.

2. A method for carrying out circuit simulation according to claim 1 wherein, when said circuit is a MOS circuit including a plurality of MOS semiconductor devices, the frequency of shifting from the source or drain of a MOS semiconductor device to the gate thereof while tracing a path linking said external terminal and a given terminal of each of said plurality of partial circuits is assessed as the intensity of influence of said external terminal.

3. A method for carrying out circuit simulation according to claim 1 wherein, when the connectional

relationships of at least ones of the corresponding input terminals and output terminals of said plurality of partial circuits to be inspected for equivalence are judged to be mutually inconsistent, a plurality of other partial circuits connected to at least ones of said input terminals and output terminals are inspected for quasi-equivalence; and when said plurality of other partial circuits are judged as quasi-equivalent circuits, said plurality of partial circuits to be inspected for equivalence are regarded to exhibit equivalent operational characteristics.

4. A method for carrying out circuit simulation according to claim 1 wherein, when a plurality of partial circuits are inspected for equivalence, a unique element having no counterpart within said circuit is detected; if a terminal that has not been judged as a unique terminal having no counterpart is included in terminals connected to said unique element, said terminal is newly judged as a unique terminal; and said plurality of partial circuits connected to said newly judged unique terminal are inspected for equivalence.

5. An apparatus for carrying out circuit simulation, comprising:

a circuit extracting unit for extracting a plurality of partial circuits, which will be inspected for equivalence in order to check if they exhibit equivalent operational characteristics, from a circuit that is an object of circuit simulation;

a storage unit for holding data concerning the configurations of said plurality of partial circuits, the connectional relationships of at least ones of the corresponding input terminals and output terminals of said plurality of partial circuits, and the operational characteristics of corresponding component elements of said plurality of partial circuits;

an assessing unit for assessing the intensify of the influence of an external terminal of

said circuit, by tracing paths linking said external terminal and given terminals of said plurality of partial circuits; and

a circuit-equivalence inspecting circuit for detecting partial circuits exhibiting equivalent operational characteristics by inspecting said plurality of partial circuits for equivalence, on the basis of the results of assessment concerning the intensity of influence of said external terminal provided by said assessing unit, and said data held by said storage unit,

wherein, after said circuit is compressed by integrating said partial circuits exhibiting equivalent operational characteristics into one circuit, circuit simulation is carried out.

6. An apparatus for carrying out circuit simulation according to claim 5 wherein, when said circuit is a MOS circuit including a plurality of MOS semiconductor devices, said assessing unit assesses, as the intensity of the influence of said external terminal, the frequency of shifting from the source or drain of a MOS semiconductor device to the gate thereof while tracing a path linking said external terminal and a given terminal of each of said plurality of partial circuits.

7. An apparatus for carrying out circuit simulation according to claim 5, further comprising a connected-circuit quasi-equivalence inspecting unit for, when said circuit-equivalence inspecting circuit judges that the connectional relationships of at least ones of the corresponding input terminals and output terminals of said plurality of partial circuits to be inspected for equivalence are mutually inconsistent, inspecting a plurality of other partial circuits connected to at least ones of said input terminals and output terminals for quasi-equivalence,

wherein when said connected-circuit quasi-equivalence inspecting unit judges that said plurality of other partial circuits are quasi-equivalent

circuits, said plurality of partial circuits to be inspected for equivalence are regarded to exhibit equivalent operational characteristics.

8. An apparatus for carrying out circuit simulation according to claim 5 wherein, when said circuit-equivalence inspecting circuit inspects a plurality of partial circuits for equivalence, it detects a unique element having no counterpart within said circuit; when a terminal that has not been judged as a unique terminal having no counterpart is included in terminals connected to said unique element, said terminal is newly judged as a unique terminal; and said plurality of partial circuits connected to said newly judged unique terminal are inspected for equivalence.

METHOD AND APPARATUS FOR CARRYING OUT CIRCUIT SIMULATION

ABSTRACT OF THE DISCLOSURE

In a method and apparatus for carrying out circuit simulation which performs circuit simulation on a circuit to be simulated, a plurality of partial circuits to be inspected for equivalence in order to check if they exhibit equivalent operational characteristics are extracted from the circuit to be simulated, and the intensity of the influence of an external terminal of the circuit to be simulated is assessed by tracing paths linking the external terminal and given terminals of the partial circuits. Moreover, based on the configurations of the partial circuits, the connectional relationships of corresponding input terminals of the partial circuits, the operational characteristics of corresponding component elements of the partial circuits, and the intensity of the influence of the external terminal, the plurality of partial circuits are inspected for equivalence in order to detect partial circuits exhibiting equivalence. After the circuit to be simulated is compressed by integrating the partial circuits into one circuit, circuit simulation is carried out.

Fig.1A

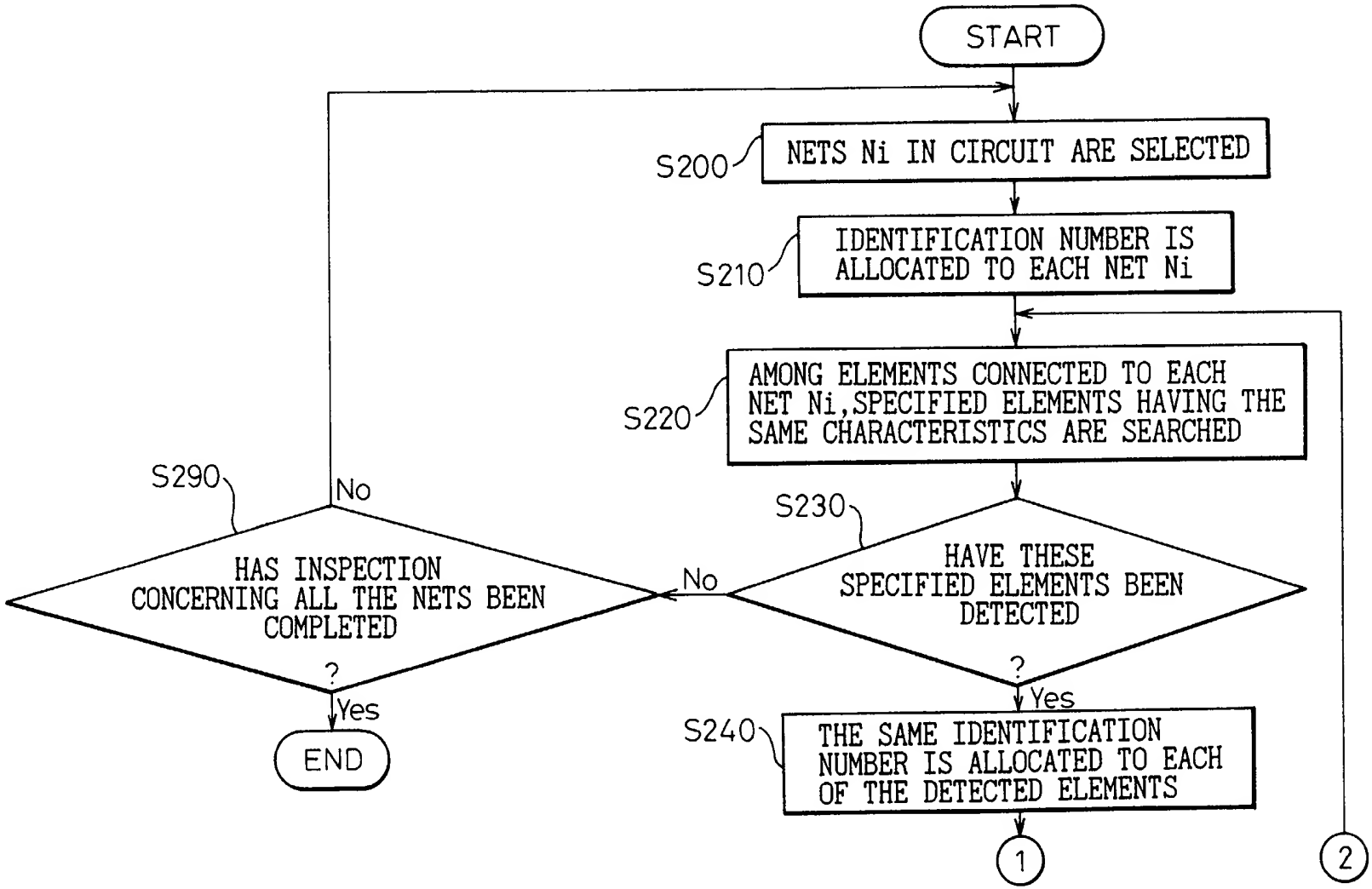

START
S200
NETS Ni IN CIRCUIT ARE SELECTED
S210
IDENTIFICATION NUMBER IS ALLOCATED TO EACH NET Ni
S220
AMONG ELEMENTS CONNECTED TO EACH NET Ni, SPECIFIED ELEMENTS HAVING THE SAME CHARACTERISTICS ARE SEARCHED
S230
HAVE THESE SPECIFIED ELEMENTS BEEN DETECTED
?
No
Yes
S240
THE SAME IDENTIFICATION NUMBER IS ALLOCATED TO EACH OF THE DETECTED ELEMENTS
1
2
S290
HAS INSPECTION CONCERNING ALL THE NETS BEEN COMPLETED
?
No
Yes
END

Fig. 1B

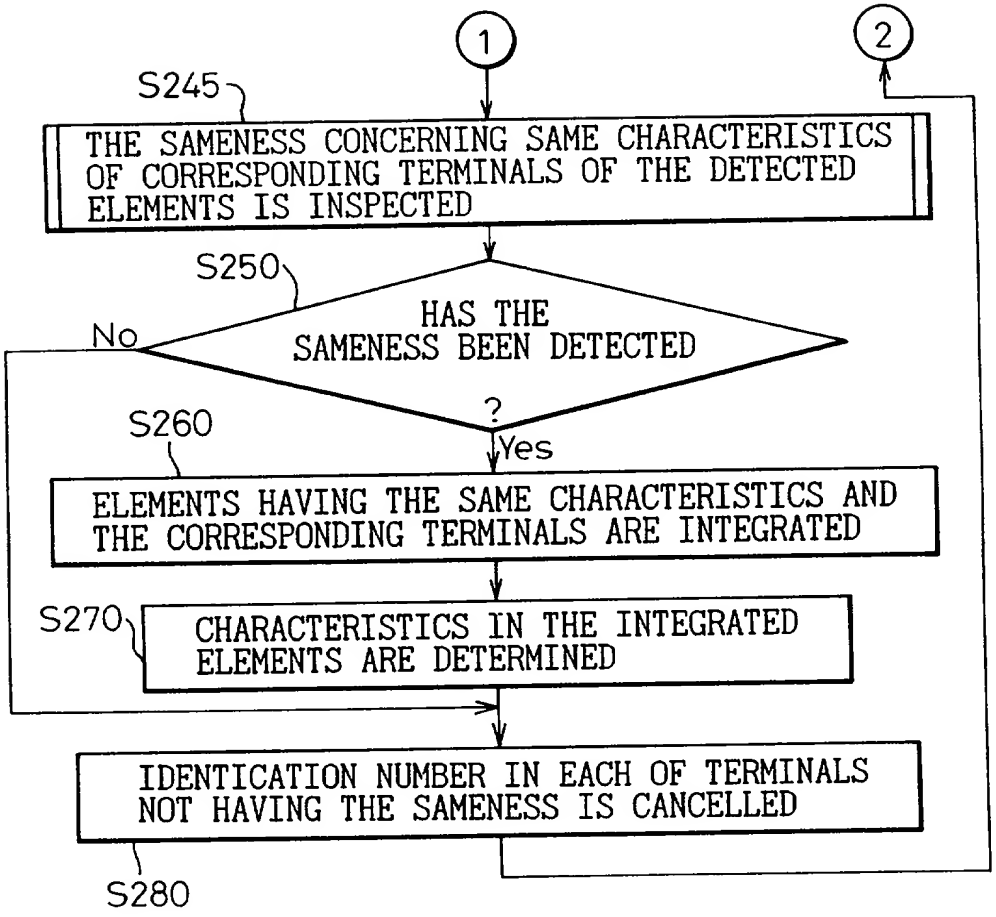

1
2
S245
THE SAMENESS CONCERNING SAME CHARACTERISTICS OF CORRESPONDING TERMINALS OF THE DETECTED ELEMENTS IS INSPECTED
S250
HAS THE SAMENESS BEEN DETECTED ?
No
Yes
S260
ELEMENTS HAVING THE SAME CHARACTERISTICS AND THE CORRESPONDING TERMINALS ARE INTEGRATED
S270
CHARACTERISTICS IN THE INTEGRATED ELEMENTS ARE DETERMINED
IDENTICATION NUMBER IN EACH OF TERMINALS NOT HAVING THE SAMENESS IS CANCELLED
S280

Fig.2

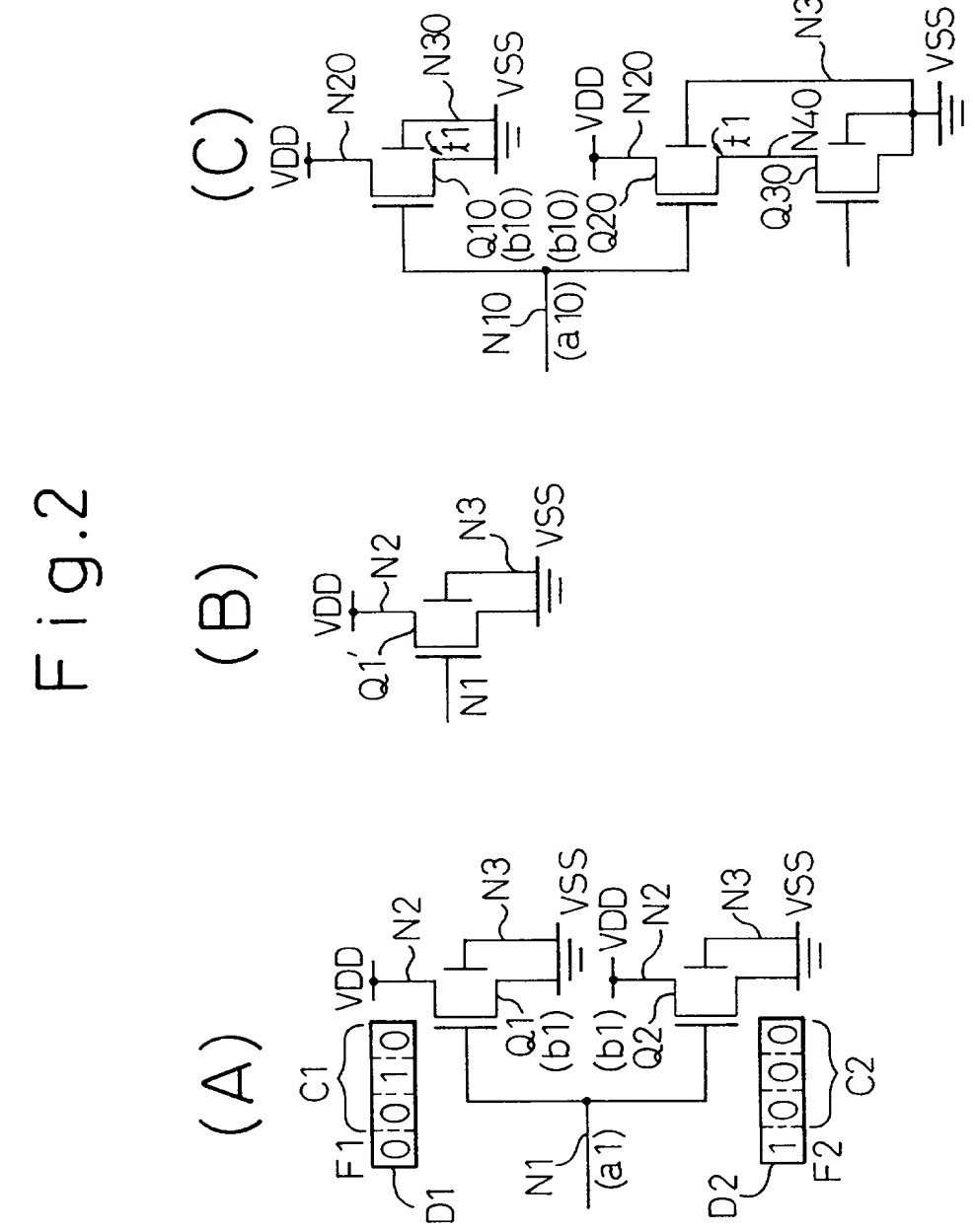

(A)
C1
F1
0:0:1:0
D1
VDD
N2
N3
VSS
Q1
(b1)
N1
(a1)
VDD
N2
(b1)
Q2
N3
VSS
D2
1:0:0:0
F2
C2
(B)
VDD
N2
Q1'
N3
VSS
N1
(C)
VDD
N20
N30
VSS
Q10
(b10)
N10
(a10)
(b10)
Q20
VDD
N20
Q30
N40
N30
VSS

Fig. 3

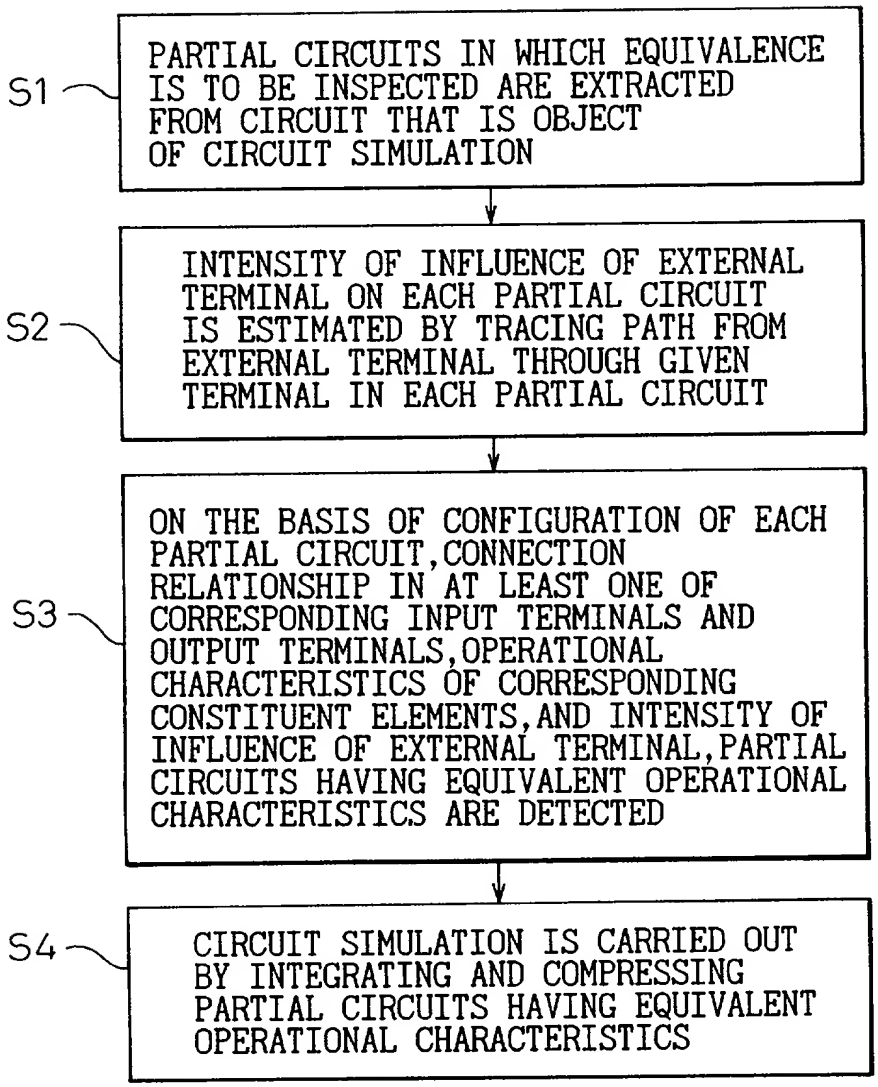

S1
PARTIAL CIRCUITS IN WHICH EQUIVALENCE IS TO BE INSPECTED ARE EXTRACTED FROM CIRCUIT THAT IS OBJECT OF CIRCUIT SIMULATION
S2
INTENSITY OF INFLUENCE OF EXTERNAL TERMINAL ON EACH PARTIAL CIRCUIT IS ESTIMATED BY TRACING PATH FROM EXTERNAL TERMINAL THROUGH GIVEN TERMINAL IN EACH PARTIAL CIRCUIT
S3
ON THE BASIS OF CONFIGURATION OF EACH PARTIAL CIRCUIT, CONNECTION RELATIONSHIP IN AT LEAST ONE OF CORRESPONDING INPUT TERMINALS AND OUTPUT TERMINALS, OPERATIONAL CHARACTERISTICS OF CORRESPONDING CONSTITUENT ELEMENTS, AND INTENSITY OF INFLUENCE OF EXTERNAL TERMINAL, PARTIAL CIRCUITS HAVING EQUIVALENT OPERATIONAL CHARACTERISTICS ARE DETECTED
S4
CIRCUIT SIMULATION IS CARRIED OUT BY INTEGRATING AND COMPRESSING PARTIAL CIRCUITS HAVING EQUIVALENT OPERATIONAL CHARACTERISTICS

Fig.4

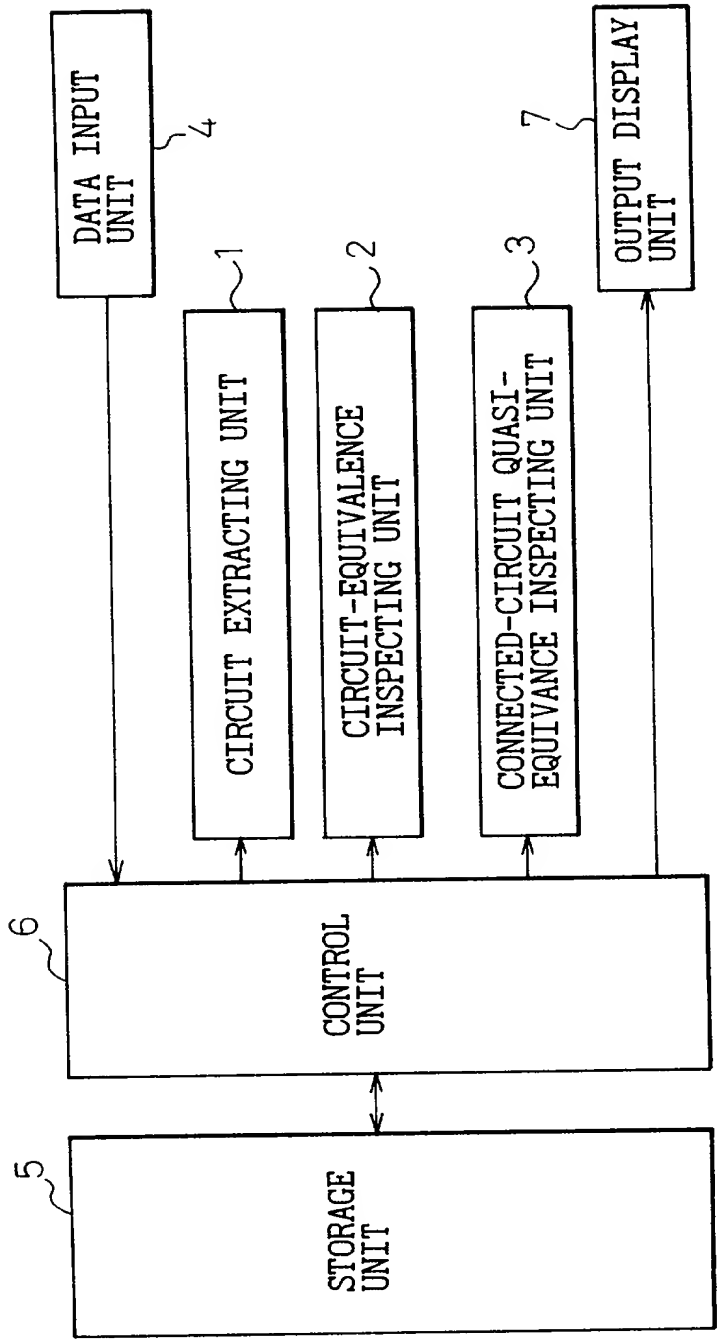

DATA INPUT UNIT
4
CIRCUIT EXTRACTING UNIT
1
CIRCUIT-EQUIVALENCE INSPECTING UNIT
2
CONNECTED-CIRCUIT QUASI-EQUIVANCE INSPECTING UNIT
3
OUTPUT DISPLAY UNIT
7
CONTROL UNIT
6
STORAGE UNIT
5

Fig.5

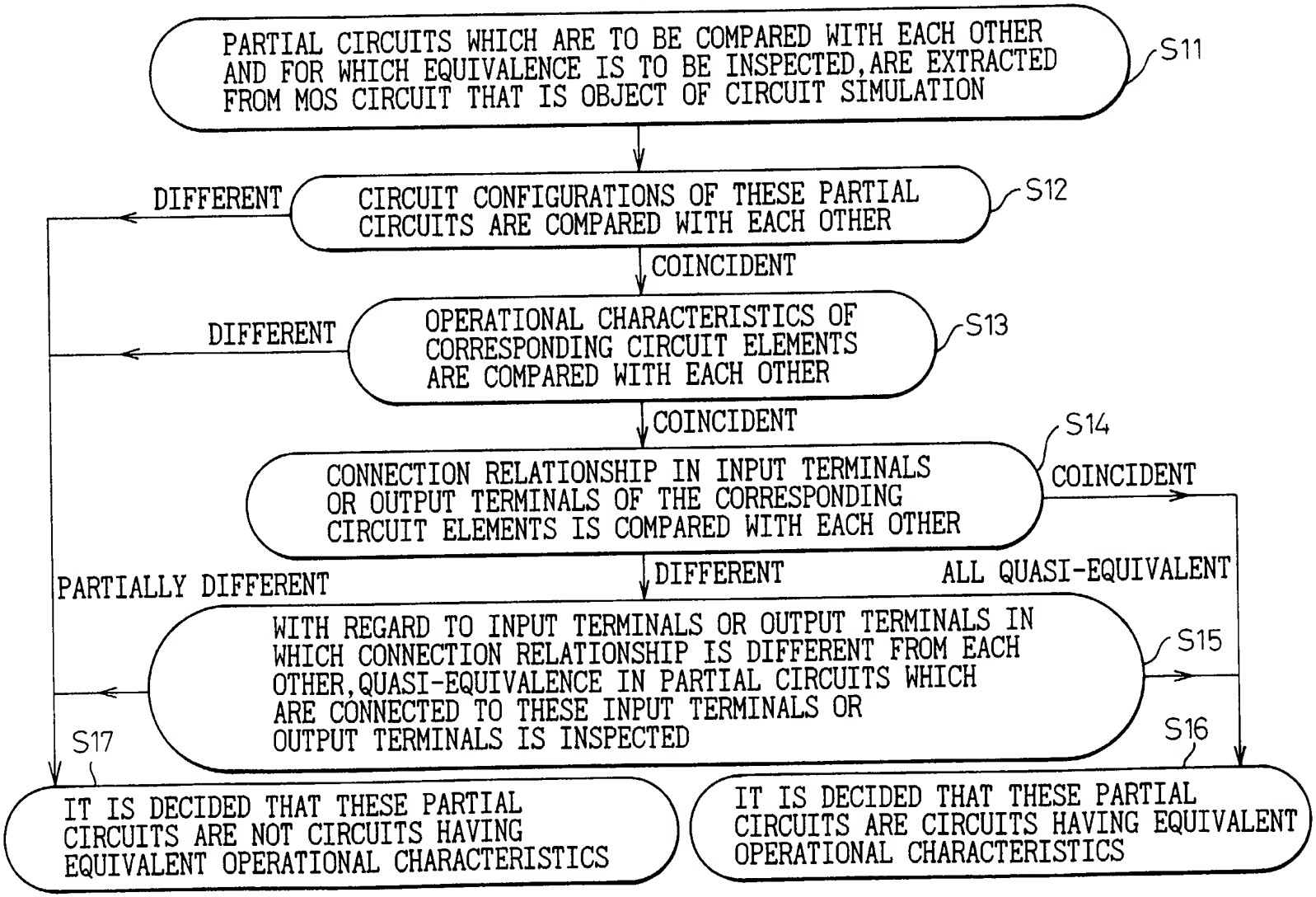

PARTIAL CIRCUITS WHICH ARE TO BE COMPARED WITH EACH OTHER AND FOR WHICH EQUIVALENCE IS TO BE INSPECTED, ARE EXTRACTED FROM MOS CIRCUIT THAT IS OBJECT OF CIRCUIT SIMULATION
S11
CIRCUIT CONFIGURATIONS OF THESE PARTIAL CIRCUITS ARE COMPARED WITH EACH OTHER
S12
DIFFERENT
COINCIDENT
OPERATIONAL CHARACTERISTICS OF CORRESPONDING CIRCUIT ELEMENTS ARE COMPARED WITH EACH OTHER
S13
DIFFERENT
COINCIDENT
CONNECTION RELATIONSHIP IN INPUT TERMINALS OR OUTPUT TERMINALS OF THE CORRESPONDING CIRCUIT ELEMENTS IS COMPARED WITH EACH OTHER
S14
COINCIDENT
DIFFERENT
PARTIALLY DIFFERENT
ALL QUASI-EQUIVALENT
WITH REGARD TO INPUT TERMINALS OR OUTPUT TERMINALS IN WHICH CONNECTION RELATIONSHIP IS DIFFERENT FROM EACH OTHER, QUASI-EQUIVALENCE IN PARTIAL CIRCUITS WHICH ARE CONNECTED TO THESE INPUT TERMINALS OR OUTPUT TERMINALS IS INSPECTED
S15
S16
S17
IT IS DECIDED THAT THESE PARTIAL CIRCUITS ARE NOT CIRCUITS HAVING EQUIVALENT OPERATIONAL CHARACTERISTICS
IT IS DECIDED THAT THESE PARTIAL CIRCUITS ARE CIRCUITS HAVING EQUIVALENT OPERATIONAL CHARACTERISTICS

Fig.6

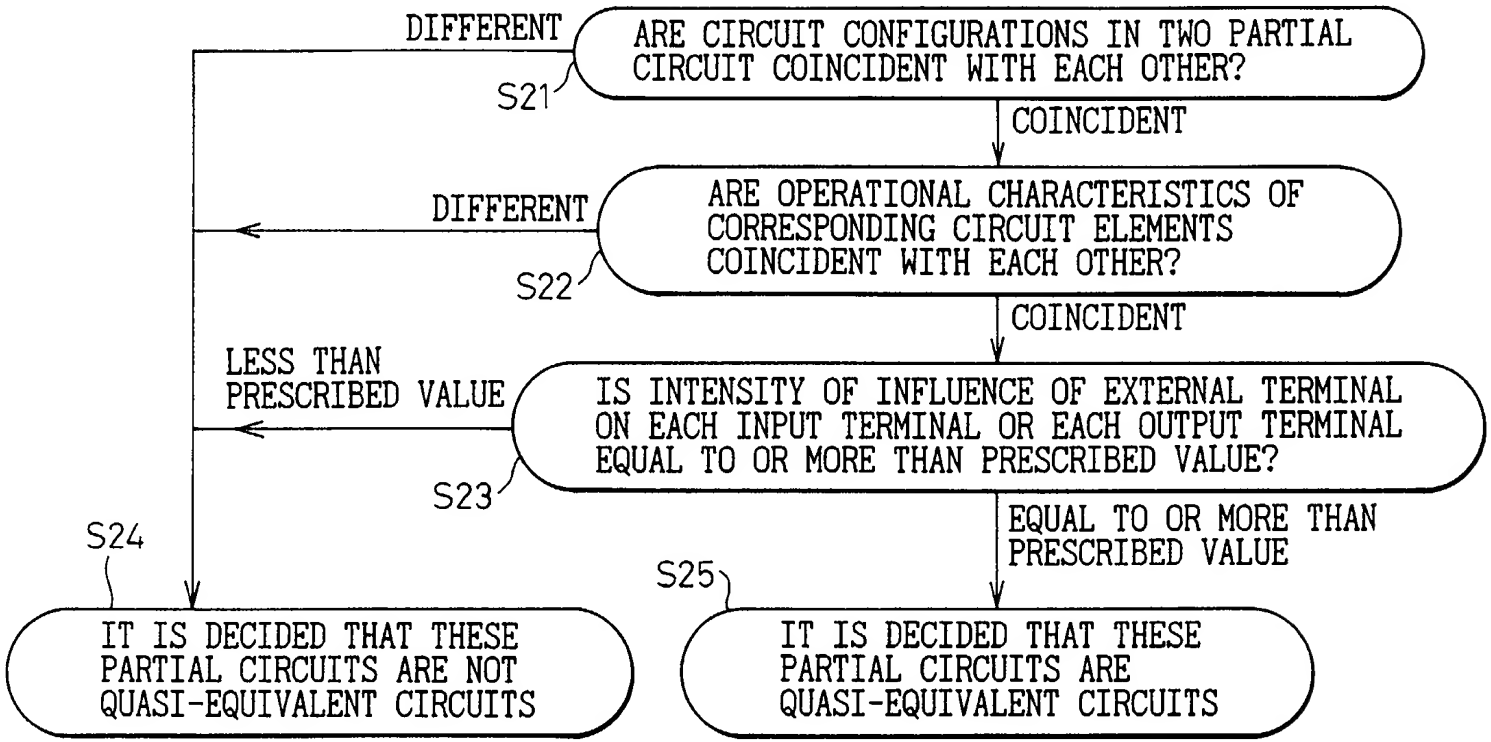

ARE CIRCUIT CONFIGURATIONS IN TWO PARTIAL CIRCUIT COINCIDENT WITH EACH OTHER?
S21
DIFFERENT
COINCIDENT
ARE OPERATIONAL CHARACTERISTICS OF CORRESPONDING CIRCUIT ELEMENTS COINCIDENT WITH EACH OTHER?
S22
DIFFERENT
COINCIDENT
IS INTENSITY OF INFLUENCE OF EXTERNAL TERMINAL ON EACH INPUT TERMINAL OR EACH OUTPUT TERMINAL EQUAL TO OR MORE THAN PRESCRIBED VALUE?
S23
LESS THAN PRESCRIBED VALUE
EQUAL TO OR MORE THAN PRESCRIBED VALUE
S24
IT IS DECIDED THAT THESE PARTIAL CIRCUITS ARE NOT QUASI-EQUIVALENT CIRCUITS
S25
IT IS DECIDED THAT THESE PARTIAL CIRCUITS ARE QUASI-EQUIVALENT CIRCUITS

Fig.7

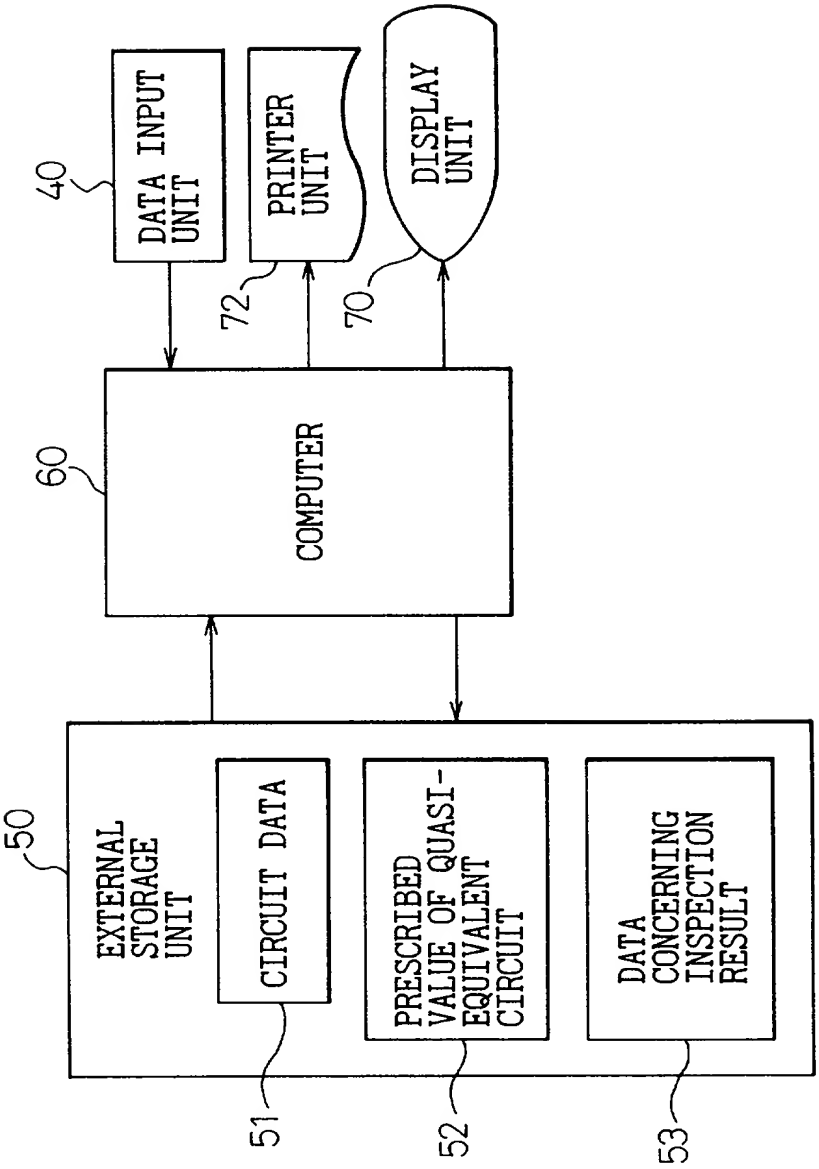

40
DATA INPUT UNIT
PRINTER UNIT
DISPLAY UNIT
72
70
60
COMPUTER
50
EXTERNAL STORAGE UNIT
CIRCUIT DATA
PRESCRIBED VALUE OF QUASI-EQUIVALENT CIRCUIT
DATA CONCERNING INSPECTION RESULT
51
52
53

Fig.8

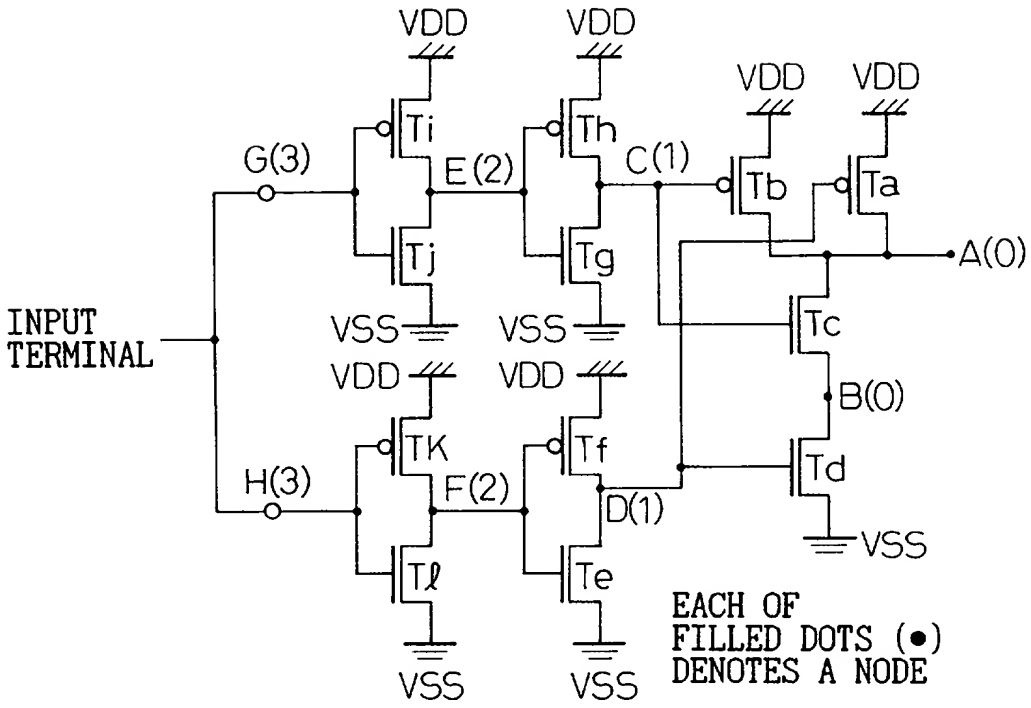

VDD
VDD
VDD
VDD
Ti
Th
Tb
Ta
G(3)
E(2)
C(1)
A(0)
Tj
Tg
INPUT TERMINAL
VSS
VSS
Tc
VDD
VDD
B(0)
TK
Tf
Td
H(3)
F(2)
D(1)
VSS
Tl
Te
EACH OF FILLED DOTS (●) DENOTES A NODE
VSS
VSS

Fig.9

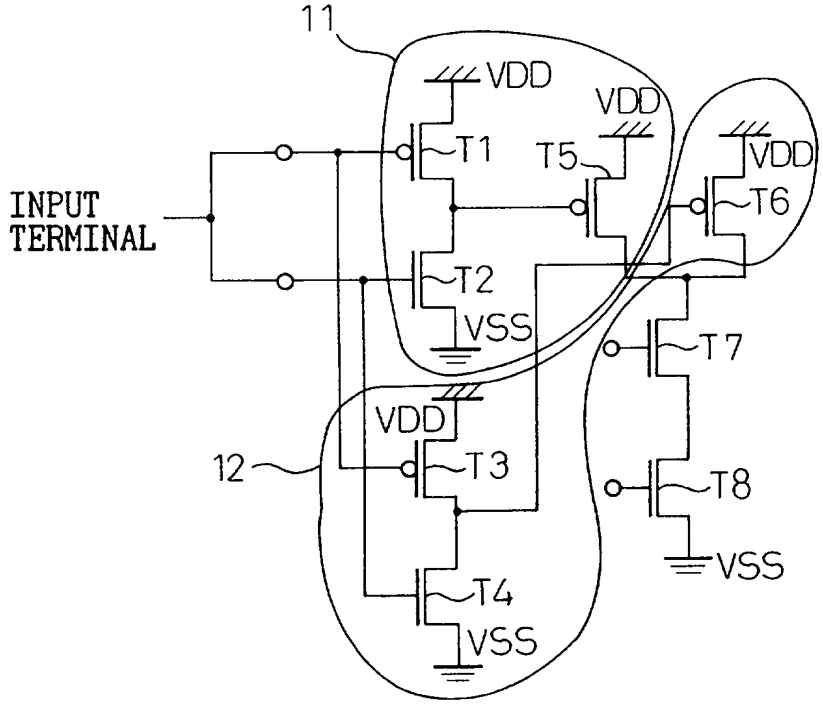

11
VDD
VDD
VDD
T1
T5
T6
INPUT TERMINAL
T2
VSS
T7
VDD
12
T3
T8
VSS
T4
VSS

Fig.10

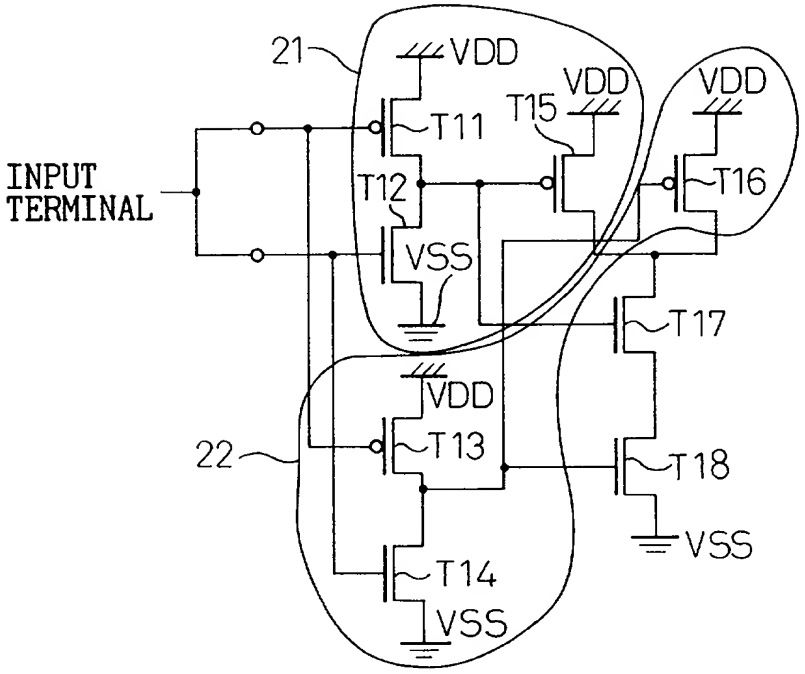

21
VDD
VDD
VDD
T15
T11
T16
INPUT
TERMINAL
T12
VSS
T17
VDD
22
T13
T18
VSS
T14
VSS

Fig.11

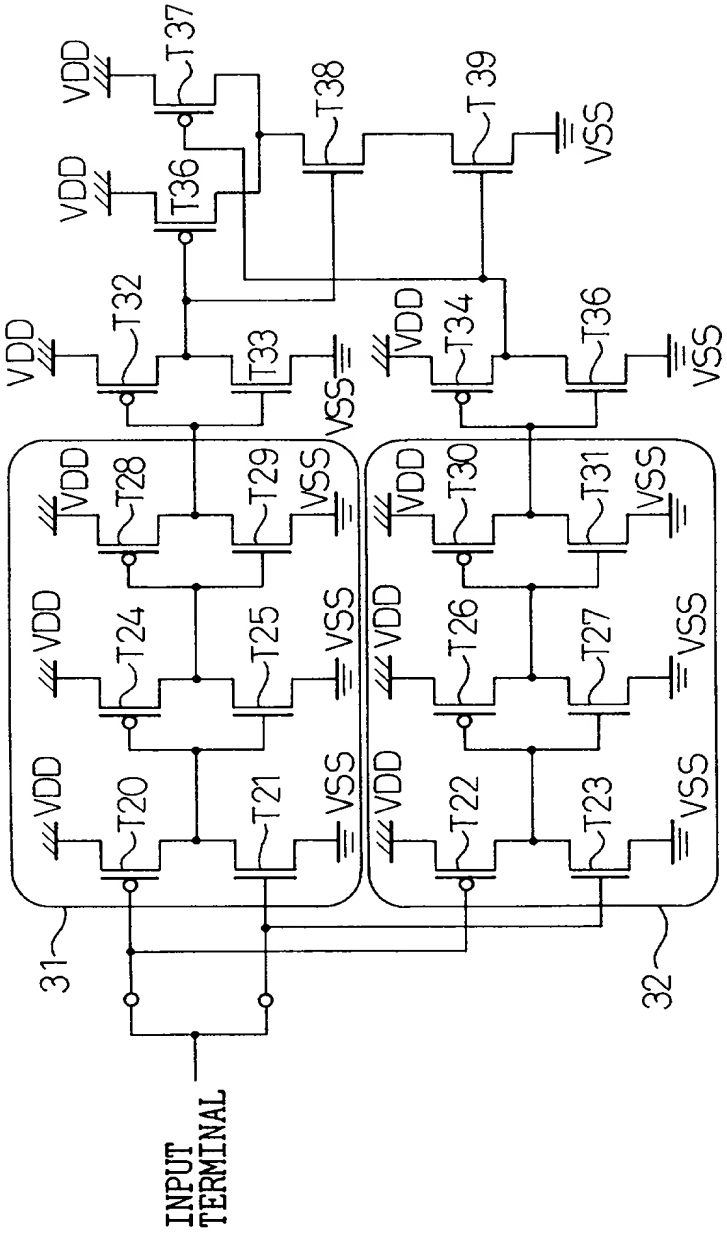

INPUT TERMINAL
31
32
VDD
VSS
T20
T21
T22
T23
T24
T25
T26
T27
T28
T29
T30
T31
T32
T33
T34
T36
T37
T38
T39

Fig.12

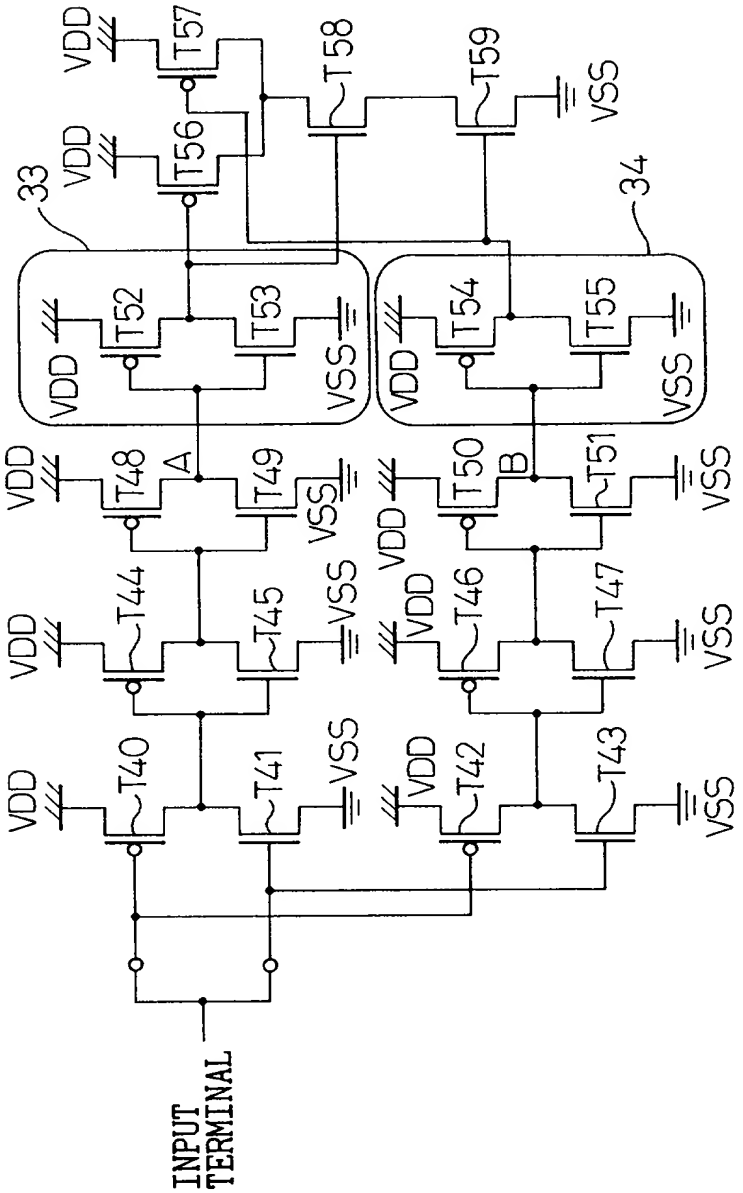

INPUT TERMINAL
VDD
VSS
T40
T41
T42
T43
T44
T45
T46
T47
T48
T49
T50
T51
T52
T53
T54
T55
T56
T57
T58
T59
A
B
33
34

Fig.13

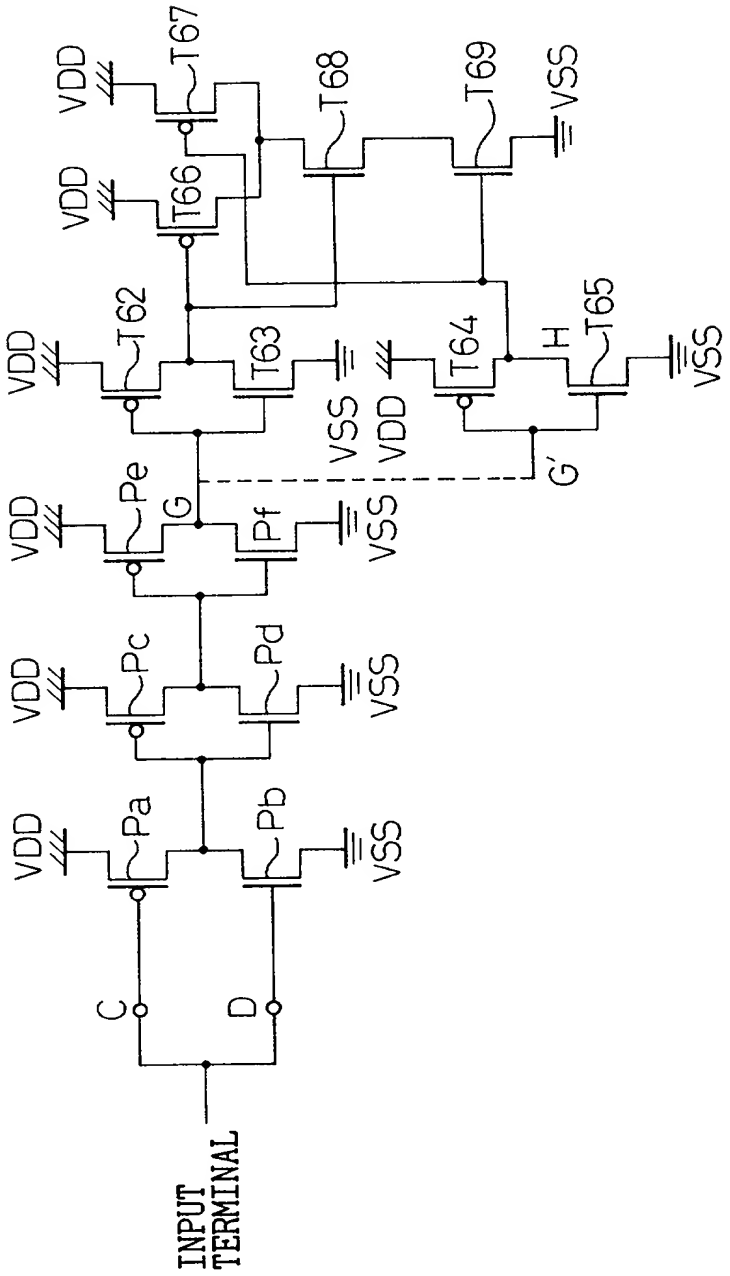
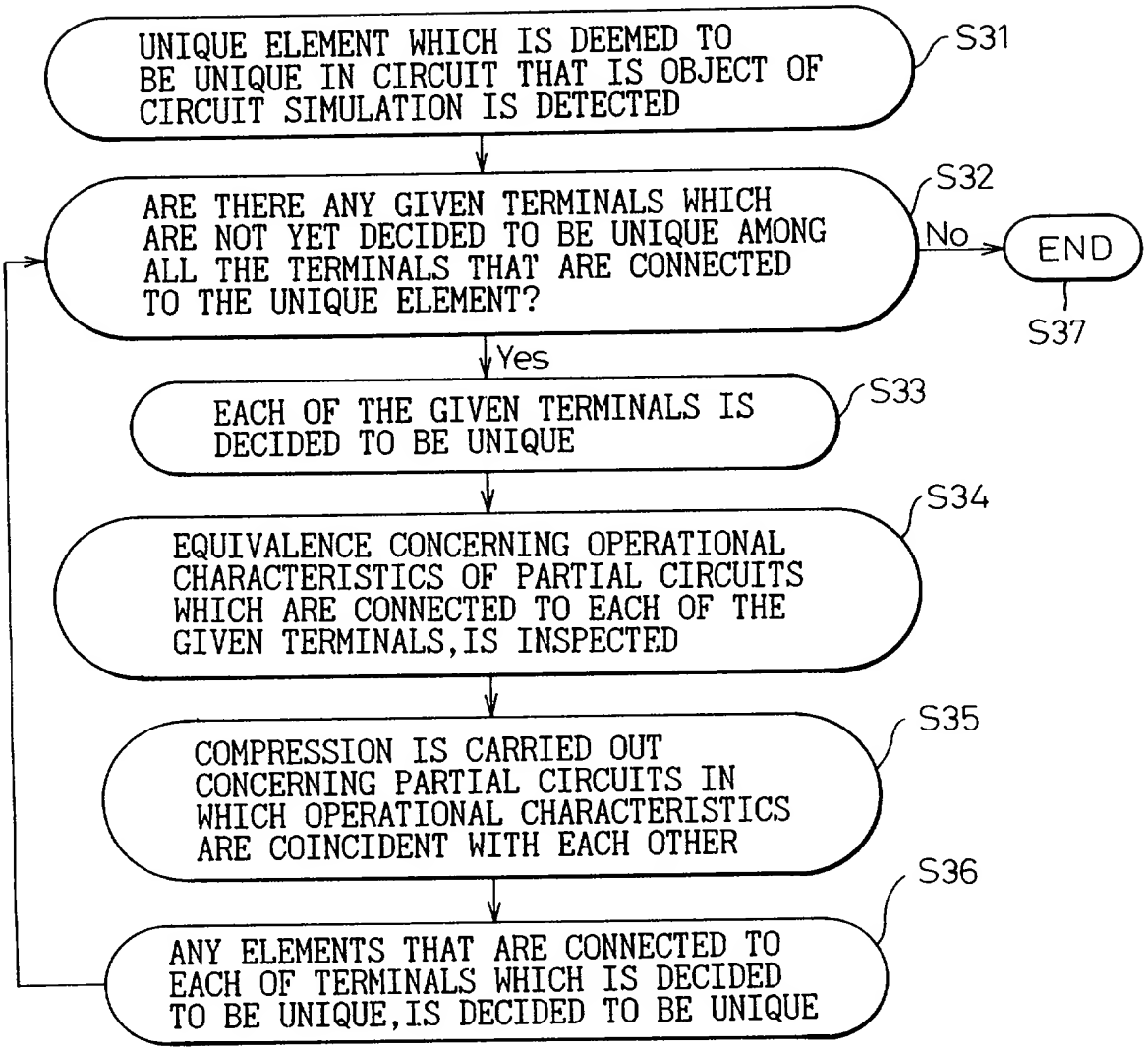

INPUT TERMINAL
C
D
VDD
Pa
Pb
VSS
Pc
Pd
Pe
Pf
G
T62
T63
T64
H
T65
T66
T67
T68
T69
G'

Fig.14


UNIQUE ELEMENT WHICH IS DEEMED TO BE UNIQUE IN CIRCUIT THAT IS OBJECT OF CIRCUIT SIMULATION IS DETECTED
S31
ARE THERE ANY GIVEN TERMINALS WHICH ARE NOT YET DECIDED TO BE UNIQUE AMONG ALL THE TERMINALS THAT ARE CONNECTED TO THE UNIQUE ELEMENT?
S32
No
END
S37
Yes
EACH OF THE GIVEN TERMINALS IS DECIDED TO BE UNIQUE
S33
EQUIVALENCE CONCERNING OPERATIONAL CHARACTERISTICS OF PARTIAL CIRCUITS WHICH ARE CONNECTED TO EACH OF THE GIVEN TERMINALS, IS INSPECTED
S34
COMPRESSION IS CARRIED OUT CONCERNING PARTIAL CIRCUITS IN WHICH OPERATIONAL CHARACTERISTICS ARE COINCIDENT WITH EACH OTHER
S35
ANY ELEMENTS THAT ARE CONNECTED TO EACH OF TERMINALS WHICH IS DECIDED TO BE UNIQUE, IS DECIDED TO BE UNIQUE
S36

PTO/SB/106 (8-96)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD AND APPARATUS FOR CARRYING OUT CIRCUIT SIMULATION

上記発明の明細書（下記の欄でx印がついていない場合は本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ _月_日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
（該当する場合）_____に訂正されました。

☐ was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Burden Hour Statement: This form is estimated to take 0.4 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner of Patents and Trademarks, Washington, DC 20231

PTO/SB/106 (8-96)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基き下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約365(a)項に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、印内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
9-186987 (Pat. Appln.)	Japan	11/July/1997	☐
			☐

私は、第35編米国法典119条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第35編120条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約365条(c)に基ずく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以後で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基ずく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基ずき、罰金または同禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の表明を行なえば、出願した、又は共に許可された特許の有効性が失われることを認識し、よってここに下記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

PTO/SB/106 (8-96)
Approved for use through 9/30/98 OMB 0651-0032
Patent and Trademark Office: U.S DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Japanese Language Declaration
(日本語宣言書)

委任状　私は下記の発明者として、本出願に関する一切の手続きを米特許商標庁に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*

James D. Halsey, Jr., 22,729; Harry John Staas, 22,010; David M. Pitcher, 25,908; John C. Garvey, 28,607; J. Randall Beckers, 30,358; William F. Herbert, 31,024; Richard A. Gollhofer, 31,106; Mark J. Henry, 36,162; Gene M. Garner II, 34,172; Michael D. Stein, 37,240; Paul I. Kravetz, 35,230; Gerald P. Joyce, III, 37,648; Todd E. Marlette, 35,269; Harlan B. Williams, Jr., 34,756; George N. Stevens, 36,938; Michael C. Soldner, P-41,455 and William M. Schertler, 35,348 (agent)

書類送付先　Send Correspondence to:

STAAS & HALSEY
700 Eleventh Street, N.W.
Suite 500
Washington, D.C. 20001

直接電話連絡先　（名前及び電話番号）　Direct Telephone Calls to: *(name and telephone number)*

STAAS & HALSEY
(202) 434-1500

唯一または第一発明者名	Full name of sole or first inventor: Hisanori Fujisawa
発明者の署名　日付	Inventor's signature: Hisanori Fujisawa　Date: March 10, 1998
住所	Residence: Kawasaki-shi, Kanagawa, Japan
国籍	Citizenship: Japanese
私書箱	Post Office Address: c/o FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8588, Japan
第二共同発明者	Full name of second joint inventor, if any
第二共同発明者　日付	Second inventor's signature　Date
住所	Residence
国籍	Citizenship
私書箱	Post Office Address

（第三以降の共同発明者についても同様に記載し、署名をすること）　(Supply similar information and signature for third and subsequent joint inventors.)